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A Charge-Sensitive Amplifier for use with Solid-State Radiation Detectors in Scientific Space Instruments

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Approved by:

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Table of Contents

List of Figures

List of Tables

Abstract

This report describes a charge-sensitive amplifier using an N-channel FET input stage. Details of the circuit configuration are discussed; and performance data with respect to noise, stability, gain variations, dynamic range, and output loading are presented.

1.0 INTRODUCTION

In February, 1964, J. H. Marshall completed work at the Jet Propulsion Laboratory (JPL) on an amplifier to be used in solid-state detector applications. This circuit, which is thoroughly described in the appendix, is the basis for the design presented in this report.

The principal reasons for modification of the original design were to improve noise performance and extend dynamic range. Since the original circuit (see Figure 3 of the appendix) used P-channel FET's at the input, it became necessary to design a conjugate circuit in order to accommodate the new low-noise N-channel FET's recently available. In addition, the output circuit required modification to provide at least 10 MeV of dynamic range at a scale factor of 1 V/MeV.

Owing to the completeness with which this generic design is analyzed in the appendix, this report will rely extensively on fundamental material from the appendix. Data, in the form of new design and performance features, will be presented in Part 2.0 (Circuit Description). Part 3.0 will present laboratory performance data, and where pertinent, will compare these data to theoretical performance.

2.0 CIRCUIT DESCRIPTION

Accuracy in charge measurements is enhanced by making the measurement independent of such parameters as source capacitance, amplifier input capacitance, and stray wiring capacitance. This basic goal is accomplished by the use of the operational amplifier configuration and is described in further detail in Reference 2.0-1.

2.0-1 ATC Staff, "An Experimenter's Handbook for Space Instrument Design," June 15, 1966, pp 78 - 85.

The amplifier described here is a high gain, broadband device with closed-loop gain and pulse shape determined by elements located in the external feedback loop. This is shown schematically in Figure 2.0-1. Initial charge integration is performed by capacitor C_{f1}, and first-order gain and pulse shaping is produced by the two equal rise and decay time constants, $R_{f2}\ C_{f2}$ and $R_{f3}\ C_{f3}$. For the case of an internal amplifier having an infinite feedback factor and infinite bandwidth, the impulse response of this network may be expressed as follows

$$\frac{V_{out}}{E} = \frac{Q_D(R_{f2} + R_{f3})}{C_{f1}\ R_{f3}} \left(\frac{t}{\tau}\right) e^{-t/\tau} \qquad (2.0\text{-}1)$$

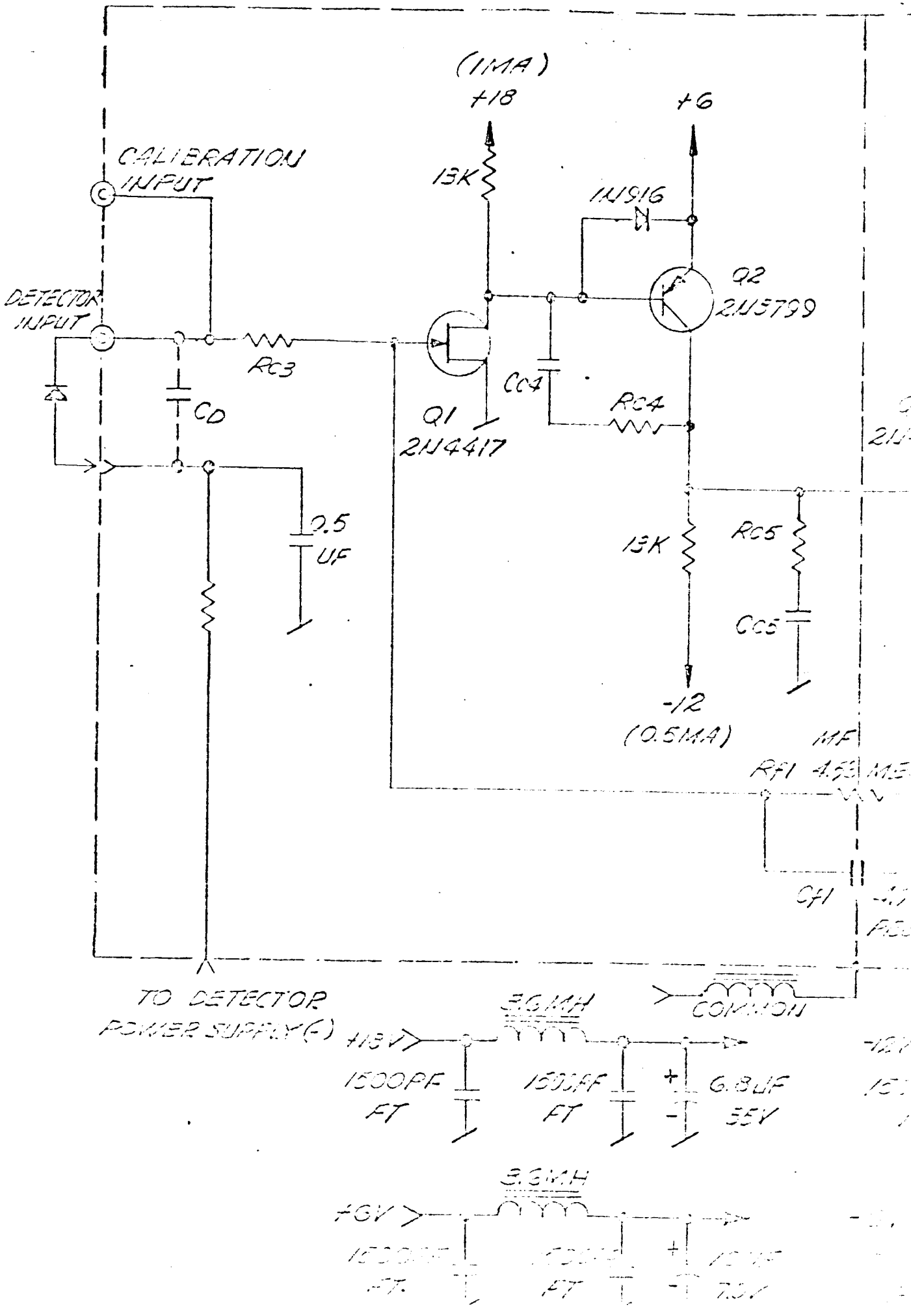
where $Q_D = 4.57 \times 10^{-17}$ C/KeV (for Silicon)

$Q_D = 5.51 \times 10^{-17}$ C/KeV (for Germanium)

τ = Shaping time constant = $R_{f2}C_{f2} = R_{f3}C_{f3}$

E = Particle energy loss

Two improvements have been made in the basic circuit, which lead to reduced input noise. One improvement is the ability to use newly available N-channel field effect transistors (FET's) at the input. A second feature is the direct coupling of the solid state detector, which permits the noise-producing bias resistor to be bypassed to ground. The pulse shaping time constant used in this study was arbitrarily chosen to be 1 μs as a possible optimization for detector current noise and amplifier voltage noise. This parameter will necessitate


(1MA)
+18
+6
CALIBRATION INPUT
13K
1N916
Q2
2N5799
DETECTOR INPUT
RC3
CC4
RC4
CD
Q1
2N4417
0.5
UF
13K
RC5
CC5
-12
(0.5MA)
MF
RF1
CF1
TO DETECTOR
POWER SUPPLY (-)
3.6MH
COMMON
+18V
1500PF
FT
1500PF
FT
6.8UF
35V
3.6MH
+6V

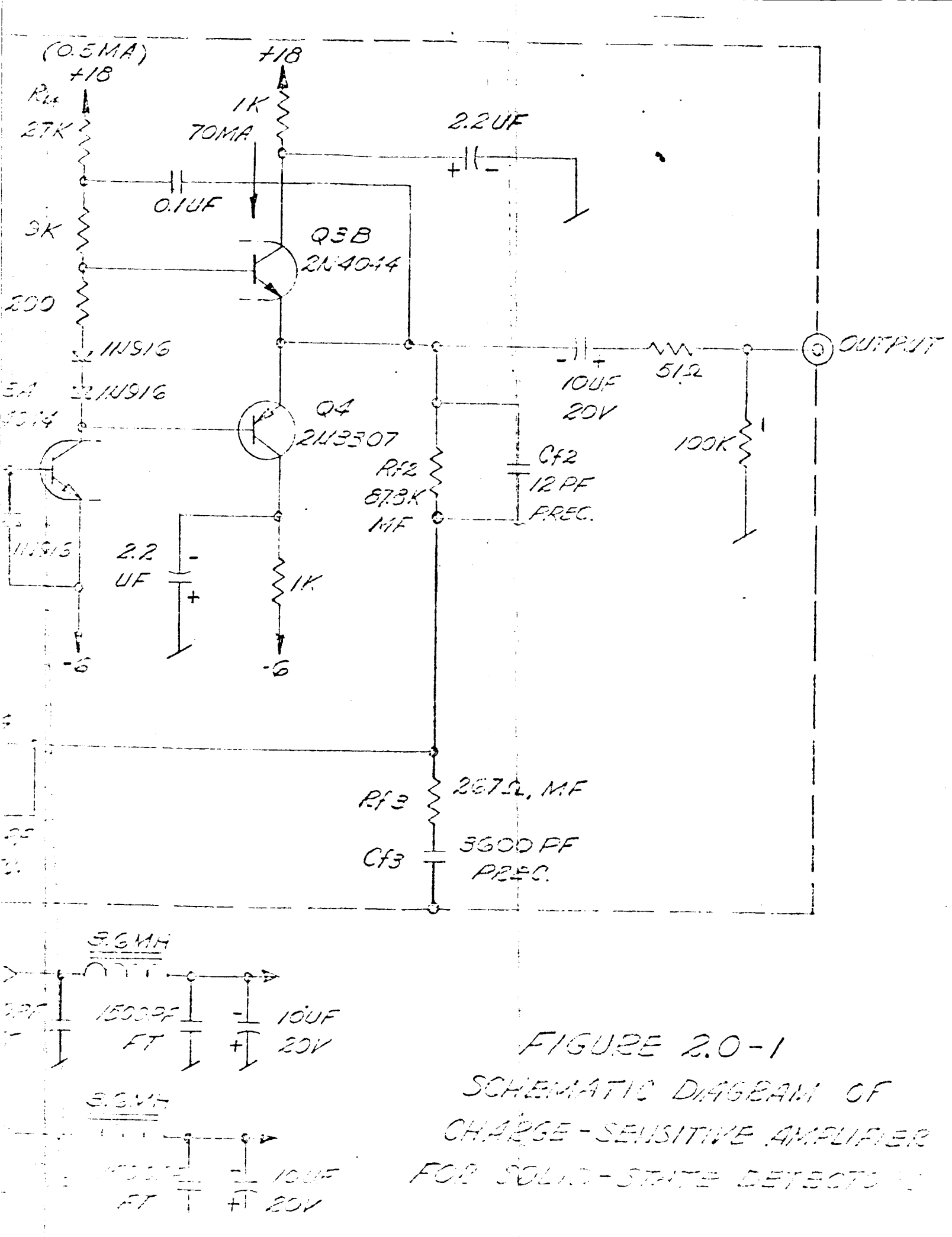


FIGURE 2.0-1

SCHEMATIC DIAGRAM OF CHARGE-SENSITIVE AMPLIFIER FOR SOLID-STATE DETECTO

additional high frequency feedback factor in order to produce the thermal gain stability obtained for the 2-μs time constant used in the circuit of the appendix.

The first stage of this four-stage direct-coupled amplifier is the N-channel FET, 2N4417, which is specified by the manufacturer to produce an equivalent input voltage noise of 3 nV/$\sqrt{\text{Hz}}$ at I_D = 1 mA. This transistor is followed by a high-gain PNP stage (2N3799). The third and last stage of voltage amplification is one half of a 2N4044 whose output is connected to a complementary emitter follower appropriately biased by the dc collector current of the third stage. This dual output stage is made up of an NPN transistor, (the other half of the 2N4044), and its PNP complement, the 2N3307. Use of the complementary circuit permits the output stage to idle at low currents and yet drive large output loads without customary loading effects of emitter bias resistors. Use of an 18-V collector supply provides an unloaded dynamic range in excess of 15 V and a response to a load of 300 pF in excess of 10 V. Large signal linearity is enhanced through the bootstrapping of Q3a load resistor to the output emitter follower. Closed loop bias levels are listed in Table 2.0-1.

Principal shaping of high frequency feedback factor is accomplished by the following networks: R_{c4} C_{c4}, R_{c5} C_{c5}, R_{c3} and the associated detector capacitance, C_D. The output network comprised of R_{c2} and C_{c2} of Figure 3 of the appendix could not be used because of rate-limiting effects under conditions of 200-pF output loading and large pulse levels.

	Location	Voltage	
Before Filter: +18.00 V	+18 V	+17.95 V	After Filter
Before Filter: +6.00	+6	+5.98	After Filter
Before Filter: -12.00	-12	-11.98	After Filter
Before Filter: -6.00	-6	-5.98	After Filter
	Q1-D	+5.35	
	Q2-C	-5.29	
	Q3b-B	-1.33	
	Q4-B	-2.60	
	Q4-E	-1.96	
	Q3b-C	+17.87	
	Q4-C	-5.91	

Table 2.0-1

Amplifier Bias Values (+25°C)

The following is a brief summary of features and advantages of this circuit:

1) The amplifier and detector circuits are direct coupled thereby eliminating secondary overshoots.

2) Direct coupling of the detector eliminates bias resistor noise.

3) Transistors are protected where required against damagingly large reverse emitter base voltages by use of protection diodes.

4) The load resistance of Q3a, the third stage voltage amplifier, is bootstrapped to the output emitter-follower thereby extending the linear operating range of the amplifier.

5) The collector circuits of the complementary output stage are capacitively decoupled to the local chassis ground thereby decoupling transient pulse loads from the power supply and other associated circuitry. All power lines are decoupled with RF filters.

6) The amplifier is partitioned into two compartments providing requisite electrostatic shielding between the output and input of the amplifier.

3.0 PERFORMANCE

This section describes results of tests on the following performance parameters: scale factor; stability against oscillation; gain stability as functions of temperature, power supply voltage and capacitive loading; and noise.

3.1 Scale Factor

For the case of infinite feedback factor, F, and equal decay and rise time constants, τ, the peak amplitude may be expressed as follows:

$$V_{peak} = \frac{Q_D}{eC_{f1}} \left(\frac{R_{f2} + R_{f3}}{R_{f3}} \right) \qquad (3.1\text{-}1)$$

where $\tau \ll \tau_{f1}$

$(\tau_{f1} = R_{f1} C_{f1})$

$e = 2.72 =$ base of natural logarithms

$Q_D = 4.57 \times 10^{-14}$ C/MeV (for silicon detectors)

In the breadboard version of Figure 2.0-1, C_{f1} consists of a stable 4.7 pF capacitance plus a distributed capacitance of approximately 1 pF measured across the 4.53 Meg parallel

resistor (R_{f1}). Taking into consideration the finite value of τ_{f1} and its associated effects, the nominal peak voltage may be rewritten as follows:

$$V_{peak} = \frac{Q_D K}{eC_{f1}} \left[1 + \frac{\tau}{\tau_{f1}} + \frac{C_{f1}}{KC_{f2}} + e^{\left(1-\frac{\tau}{\tau_{f1}}\right)} \left(\frac{1}{K} - \frac{\tau}{\tau_{f1}} \right) \right] \quad (3.1\text{-}2)$$

where

$$K = \left(\frac{R_{f2} + R_{f3}}{R_{f3}} \right) = 330$$

$$\tau_{f1} = 25.8\ \mu s$$

$$\tau = 1\ \mu s$$

and $V_{peak} = .975\ [.947] = .92$ V/MeV.

The experimentally measured scale factor was .875 V/MeV.

3.2 Stabilization Against Oscillation

As mentioned in the appendix, low gain drift (requiring large feedback factor) and a large margin of safety against oscillation are competing requirements, which require accurate prediction of oscillatory conditions in order that the design may be optimized. The problem of preserving gain stability and oscillation margins is increased further as the pulse shaping time constant, τ, is decreased because there is a greater dependence on high-frequency feedback factor.

A second constraint introduced by the smaller pulse-shaping time constant and the increased dynamic range requirement, is that capacitive networks such as R_{c2} C_{c2} in figure 3.2-1 should not be placed at the output or on the bootstrapped driver for adjustment of high-frequency feedback factor. This requirement is due to the necessity of driving load capacitances up to 200 pF without rate limiting occurring in the collector circuit of Q3a. The capacitive loading factor leaves little room for capacitive network adjustments at the output. The network comprising C_{c6} and R_{c6} would similarly add to rate limit problems and was consequently not used.

The networks consisting of R_{c5} C_{c5} and R_{c3} and C_D are suitable for such adjustments. The shunt connected network C_{c1} and R_{c1} is suitable for compensation so long as the capacitive reactance, $X_{C_{c1}} >> R_{L1}$, where R_{L1} is the first-stage drain driving point resistance, and the frequencies of interest are within the effective pass band of the closed-loop amplifier. For $X_{C_{c1}} << R_{L1}$, the second-stage voltage noise (see figure 3.2-2a) reflected to the input becomes

$$e_{n1}(f[e_{n2},C_{c1}]) = \frac{e_{n2}}{X_{C_{c1}}\, g_{m1}} . \qquad (3.2\text{-}1)$$

Miller-type compensation (figure 3.2-2b) produces an equivalent input noise,

$$e_{n1}(f[e_{n2},C_{c4}]) = \frac{e_{n2}}{X_{C_{c4}}\, g_{m1}} . \qquad (3.2\text{-}2)$$

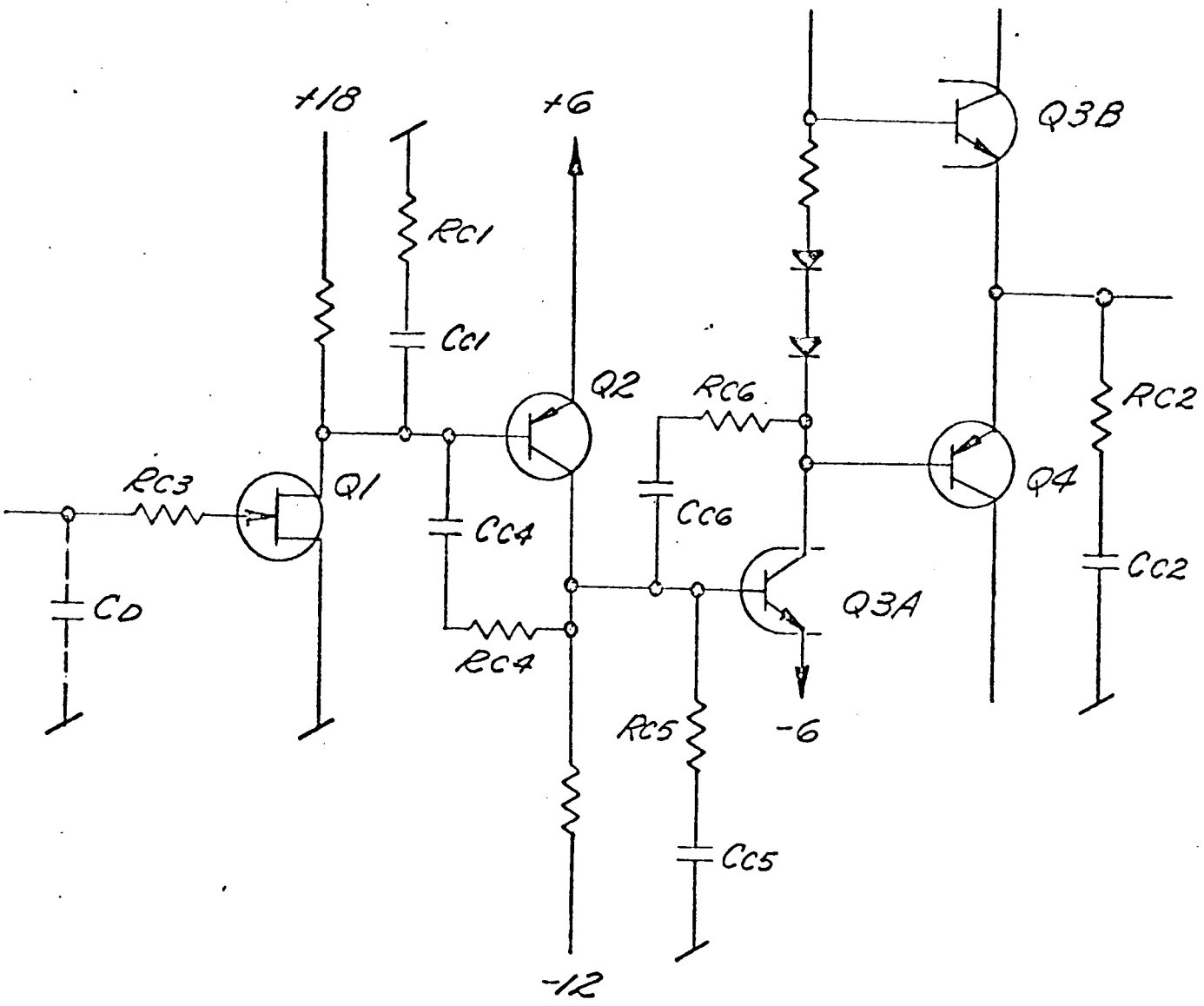
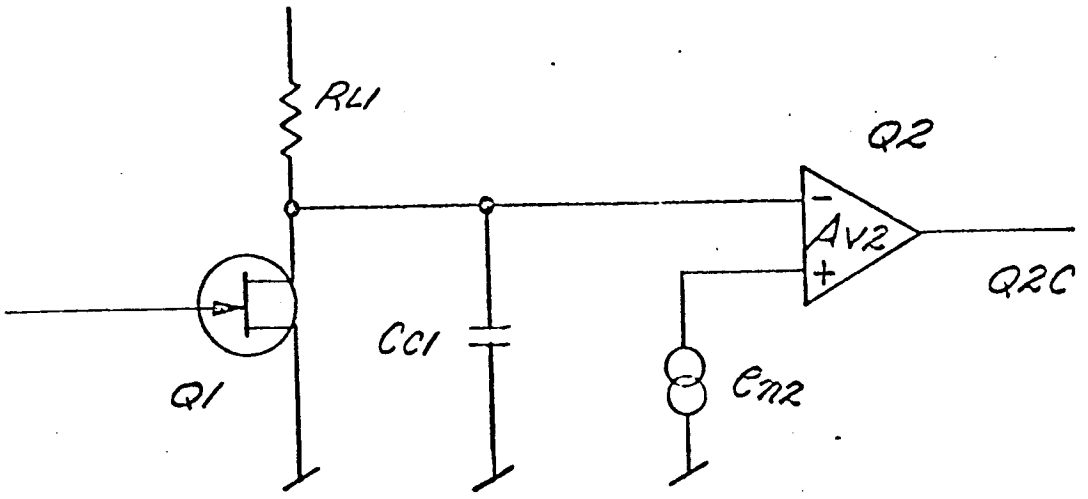
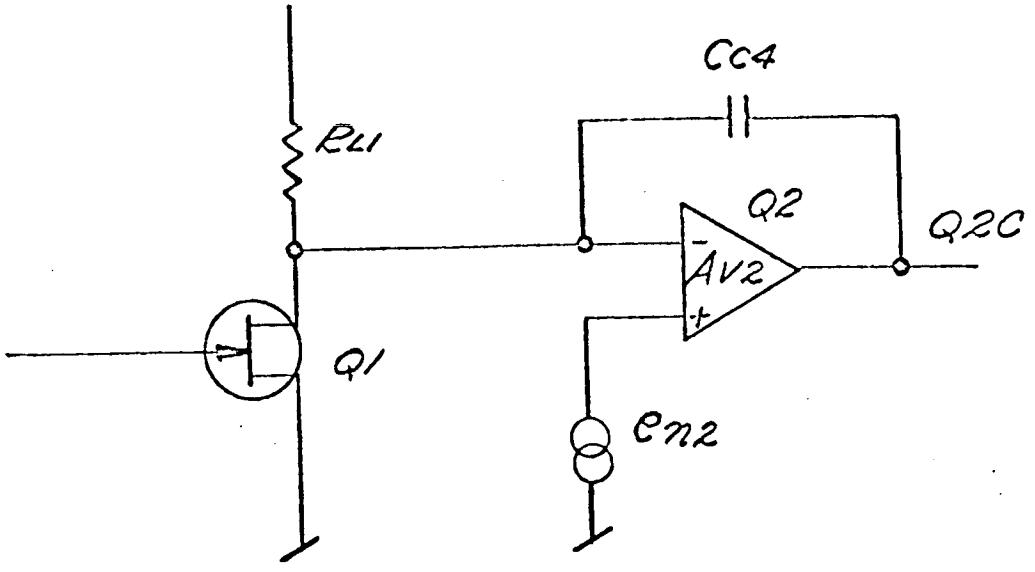


FIGURE 3.2-1

FEEDBACK SHAPING NETWORK ALTERNATIVES



a.) SHUNT CAPACITOR COMPENSATION



b.) MILLER CAPACITOR COMPENSATION

FIGURE 3.2-2

SECOND - STAGE

ROLL-OFF ALTERNATIVES

The value of C_{c4} producing a similar roll-off to that produced by C_{c1} is approximately equal to C_{c1}/A_{v2}, where A_{v2} is the second-stage voltage gain. Therefore

$$e_{n1}(f[e_{n2}, C_{c4}]) = \frac{e_{n2}}{g_{m1} A_{v2} X_{C_{c1}}} . \qquad (3.2\text{-}3)$$

For situations requiring compensation at the FET drain, the Miller-connected capacitor consequently provides best rejection to second-stage voltage noise. This connection requires that the capacitor have a sufficiently large value to be practical ($C_{c4} \geq 1$ pF). The second-stage noise rejection requirement is very similar to that of the over-all charge-sensitive amplifier. The preferability of the Miller connection as described here is, likewise, an argument, from a voltage noise standpoint, for the basic over-all configuration used here for charge-sensitive amplification.

Since primary goals of this study were to reduce noise and increase dynamic range, only rudimentary stabilization was performed to permit timely evaluation of these parameters. From this standpoint the feedback factor vs. frequency characteristic is far from optimum and is subject to considerable improvement. The following feedback factor data represent one such conservative amplifier stabilization at a detector capacitance of 100 pF. The stabilization parameters for this illustration are

C_{c4} = 20 pF

R_{c4} = 510 Ω

R_{c3} = 200 Ω

The feedback factor may be written as follows:

$$F = F_o \left\{ \frac{(1+p\tau_{f1})(1+p\tau)^2(1-p\tau_j)(1+p\tau_L)(1+p\tau_{c3})(1+p\tau_{c4})}{(1+p\tau_A)(1+p\tau_B)(1+p\tau_C)(1+p\tau_D)(1+p\tau_E)(1+p\tau_F)(1+p\tau_G)} \right.$$

$$\left. \frac{}{(1+p\tau_H)(1+p\tau_I)(1+p\tau_K)(1+p\tau_{c7})(1+p\tau_M)} \right\} \qquad (3.2\text{-}4)$$

where

p = Laplace operator

and F_o = DC feedback factor

The parameters of equation 3.2-4 have been calculated with the assistance of equations appearing on pages 14 to 17 of the appendix. The pertinent transistor parameters are listed in Table 3.2-1, and the calculated gain and time constants are shown in Table 3.2-2. As a result of certain differences between the circuit described in this report and that of Appendix A, the following new or modified relationships have been used:

1) $$M_{V3} = \frac{r_{oe}}{r_e} = \frac{2 \times 10^5}{50} = 4 \times 10^3 \qquad (3.2\text{-}5)$$

This modification occurs as a result of the bootstrapped load resistance being much larger than the transistor output resistance.

	2N4417	2N3799	2N4044	2N3307
V_{CEO} or V_{DGO} Max.	30 V	60 V	60 V	35 V
h_{FE} @ 25°C, 1 mA: min/max	——	300/900	225/675	40/250
g_m @ 1 mA	2240 µmhos	——	——	——
C_{ob}, pF	1	4	0.8	1
C_{ib}, pF	3.5	8	1	——
C_{c-c}, pF	——	——	0.8	——
f_T @ 1 mA, Hz	——	100×10^6	200×10^6	——
f_T @ .5 mA, Hz	——	30×10^6	——	——
f_T @ 2 mA, Hz (min/max)	——	——	——	$300/1200 \times 10^6$
Noise, $nV/\sqrt{Hz}$	3	——	——	——

Table 3.2-1

Transistor Parameters

(Note: Vacant spaces represent non-applicable or unavailable data)

Table 3.2-2

Feedback Factor Time Constants

ITEM	C_D = 100 pF, C_{c4} = 20 pF	
	C_L = 200 pF	C_L = 0
$F_o \times 10^7$	1.28	1.28
τ_A, μs	565	565
τ_B, μs	322	322
τ_C, ns	278	278
τ_D, ns	4.45	4.45
τ_E, ns	624	520
τ_F, ns	50	3
τ_G, ns	10*	10*
τ_H, ns	10*	10*
τ_I, ns	1.54	1.54
τ_J, ns	0.2	0.2
τ_K, μs	317	317
τ_L, ns	10	———
τ, μs	1	1
τ_{f1}, μs	23	23
τ_{c3}, ns	20	20
τ_{c4}, ns	10	10
τ_{c7}, ns	1	1
τ_M, ns	0.6	———

(*estimated)

2) $$\tau_c = \frac{\tau_3}{1 + \frac{M_{V1}\, C_{gd}\, \tau_1}{(C_B+C_D)(\tau_2+\tau_3)}} \qquad (3.2\text{-}6)$$

where

$$\tau_3 = \frac{R_{L1}[\tau_1(C_{e2}+C_{ob2}+C_{c4}+C_{gd}) + \tau_4 M_{V2}(C_{ob2}+C_{c4})]}{\tau_2 + \tau_3} \qquad (3.2\text{-}7)$$

$$\tau_2 + \tau_3 = \tau_1 + R_{L1}\,[M_{V2}(C_{ob2}+C_{c4}) + C_{e2}] \qquad (3.2\text{-}8)$$

3) Calculation of τ_E, τ_F, τ_L, τ_M:

$$\frac{E_o'}{i_3} \cong r_{oe3}\left\{\frac{(1 + p\tau_L)}{\left\{p^2(C_L+C_{f2})(R_s+r_{e4})\tau_s + p\left[\tau_s + (C_L+C_{f2})\left(R_s + r_{e4} + \frac{r_{oe3}}{\beta_4}\right)+1\right]\right\}(1+p\tau_M)}\right\} \qquad (3.2\text{-}9)$$

(See Figure 3.2-3)

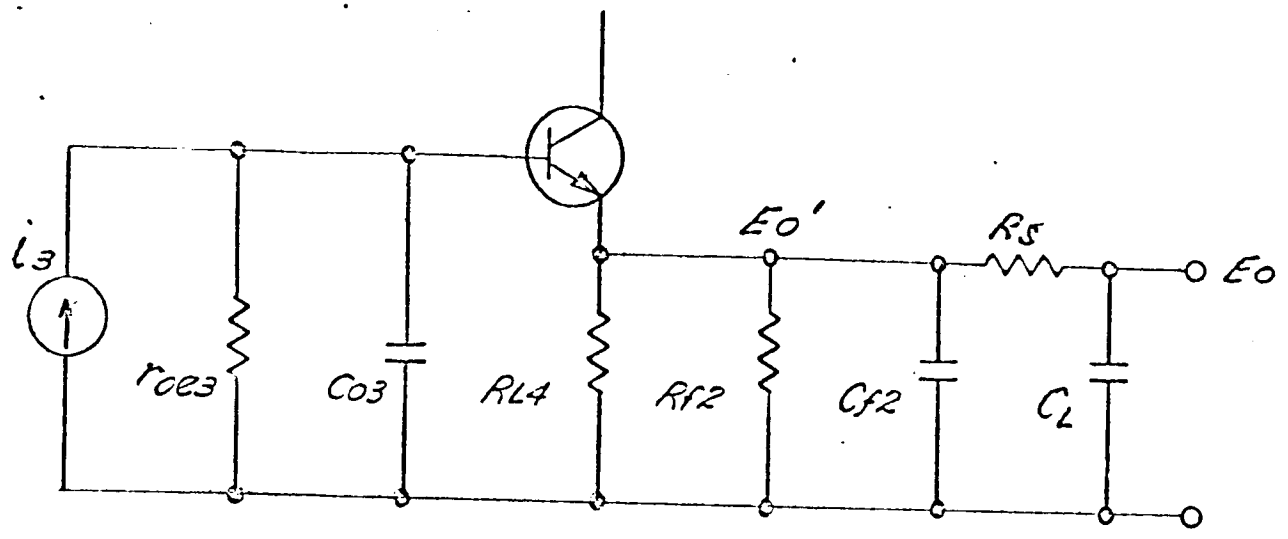
where

$$\tau_L = C_L R_s$$

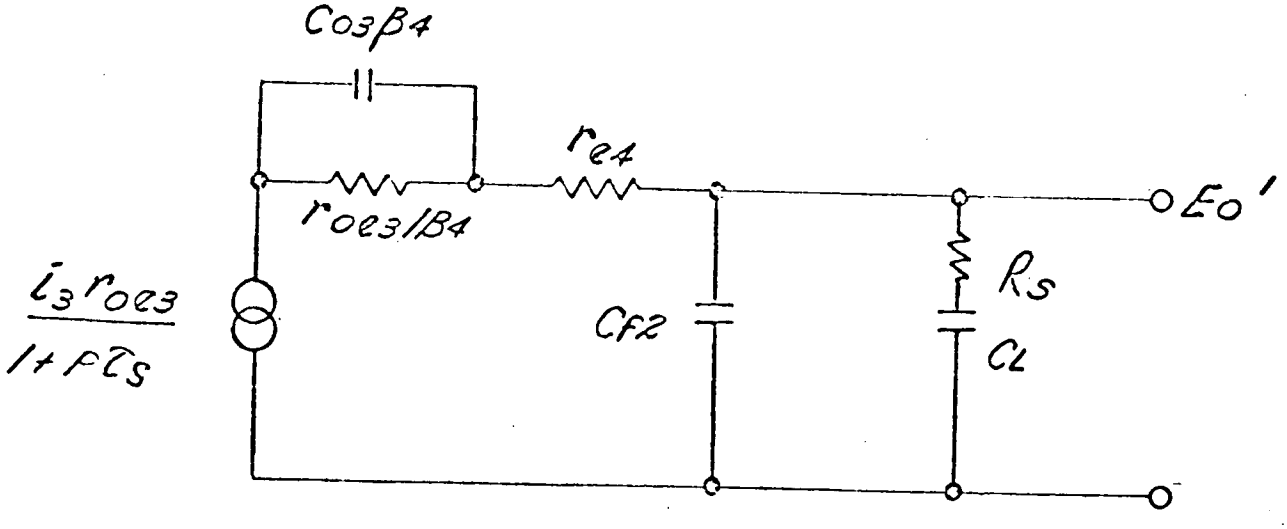
$$\tau_s = r_{oe3} C_{o3}$$

$$C_{o3} = C_{ob3A} + C_{ob3B} + C_{ob4} + \text{distributed excess}$$

$$\tau_M = R_s \frac{C_{f2}\, C_L}{C_{f2} + C_L}$$



a) EQUIVALENT AC CIRCUIT



b) APPROXIMATE EQUIVALENT OUTPUT CIRCUIT

FIGURE 3.2-3

EQUIVALENT OUTPUT CIRCUITS

Equation 3.2-9 may be factored into the form

$$\frac{E_o'}{i_3} \cong r_{oe3} \frac{1 + p\tau_L}{(1+p\tau_E)(1+p\tau_F)(1+p\tau_M)} \qquad (3.2\text{-}10)$$

where

$$\tau_E, \tau_F = \frac{2A}{B \mp \sqrt{B^2 - 4AC}}$$

where

$$A = (C_L + C_{f2})(R_s + r_{e4})\,\tau_s$$

$$B = \tau_s + (C_L + C_{f2})(R_s + r_{e4} + r_{oe3}/\beta_4)$$

For the case of $C_L = 0$,

$$\tau_E \cong \tau_s$$

$$\tau_F \cong r_{e4}C_{f2}$$

4) $\tau_{c7} = R_{c4}C_{ob2}$

A Bode plot of feedback factor using the data from Table 3.2-2 is shown in Figure 3.2-4 and indicates a no-load gain crossover at 160 ns. This response can be broadened as desired to obtain better pulse peak stability. Principal adjustments should be in τ_B, τ_C, $\tau_{C_{c3}}$ and $\tau_{C_{c4}}$.

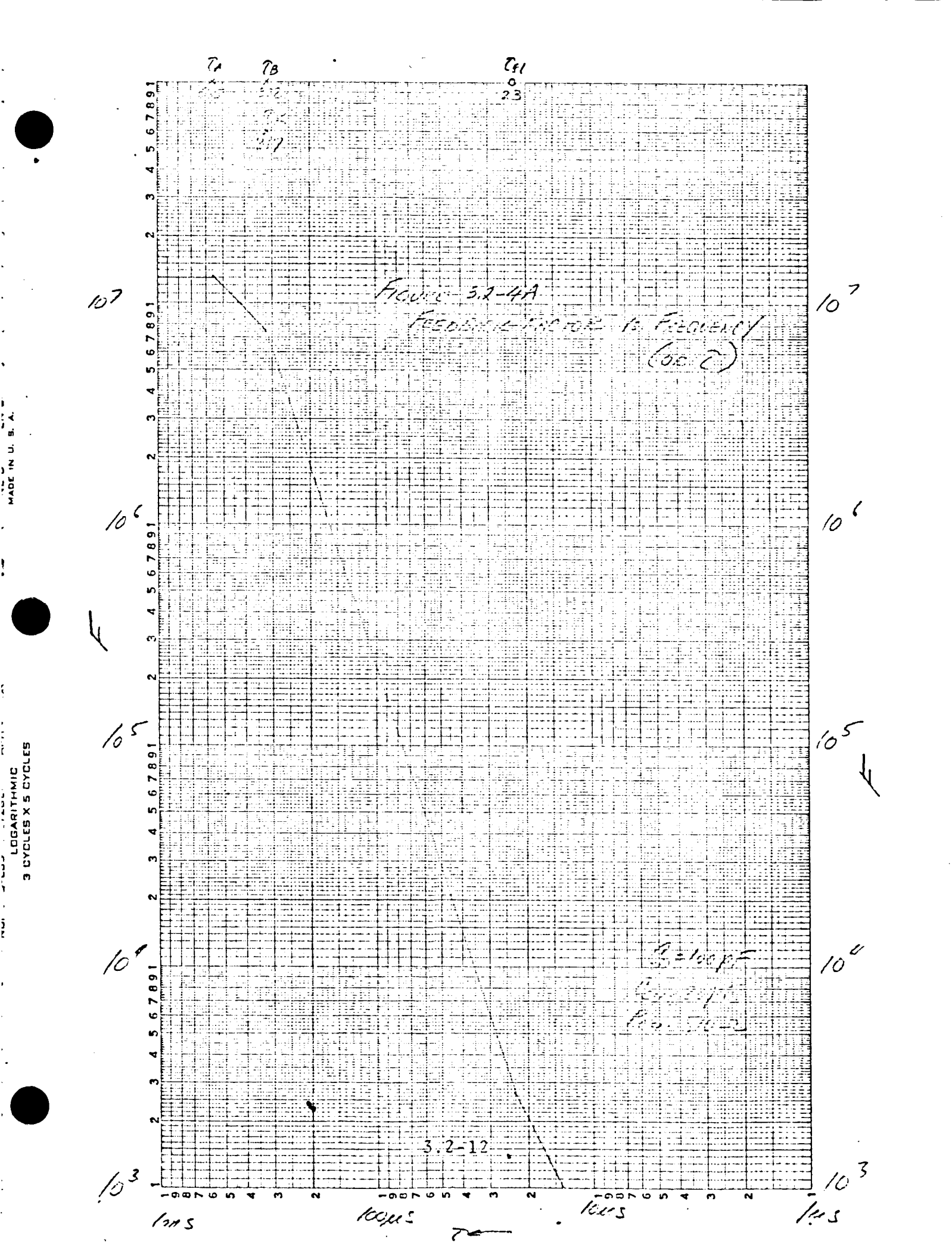
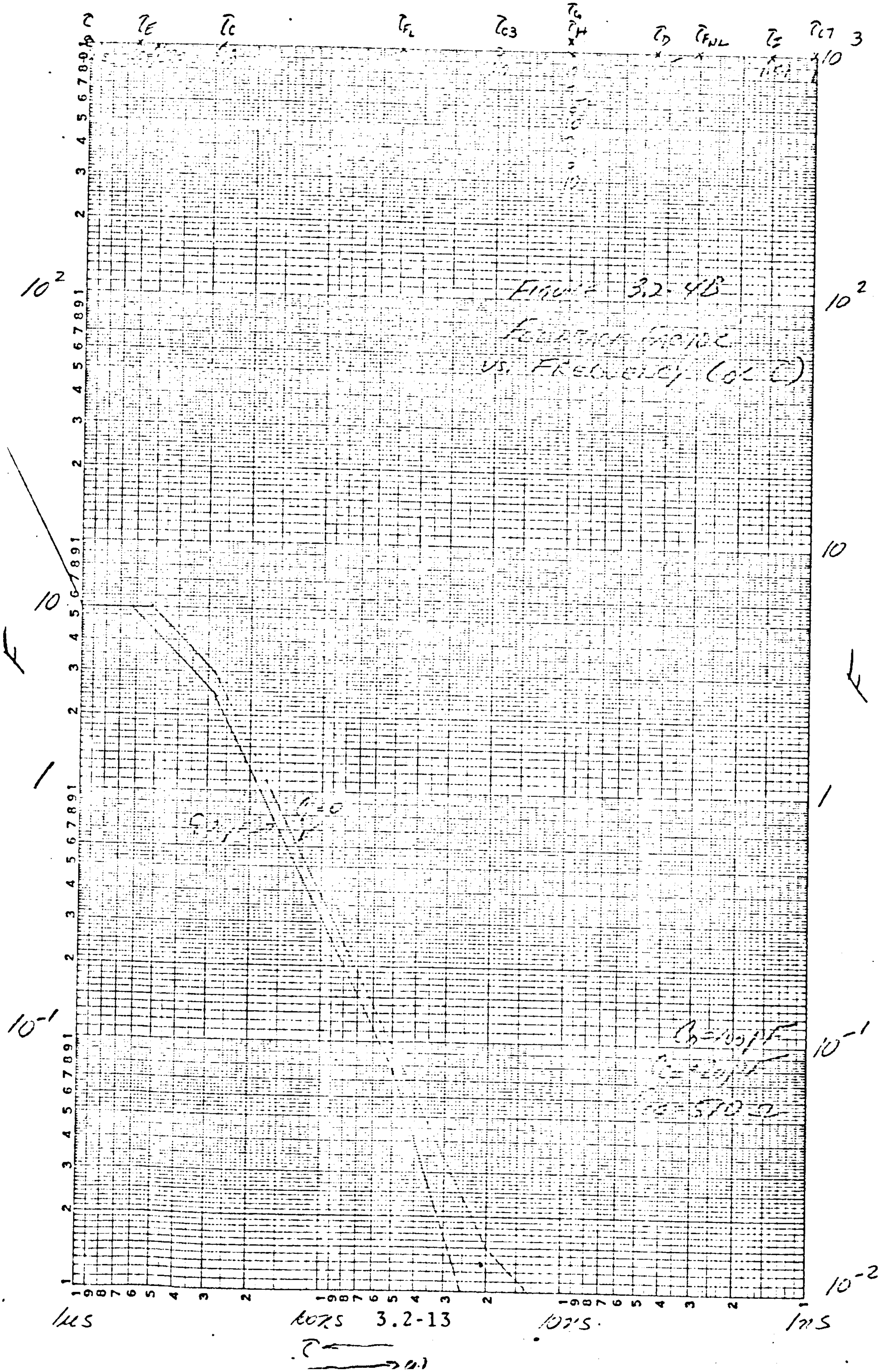


FIGURE 3.2-4A
FEEDBACK FACTOR VS. FREQUENCY
(OC C)
LOGARITHMIC
3 CYCLES X 5 CYCLES
MADE IN U. S. A.
3.2-12



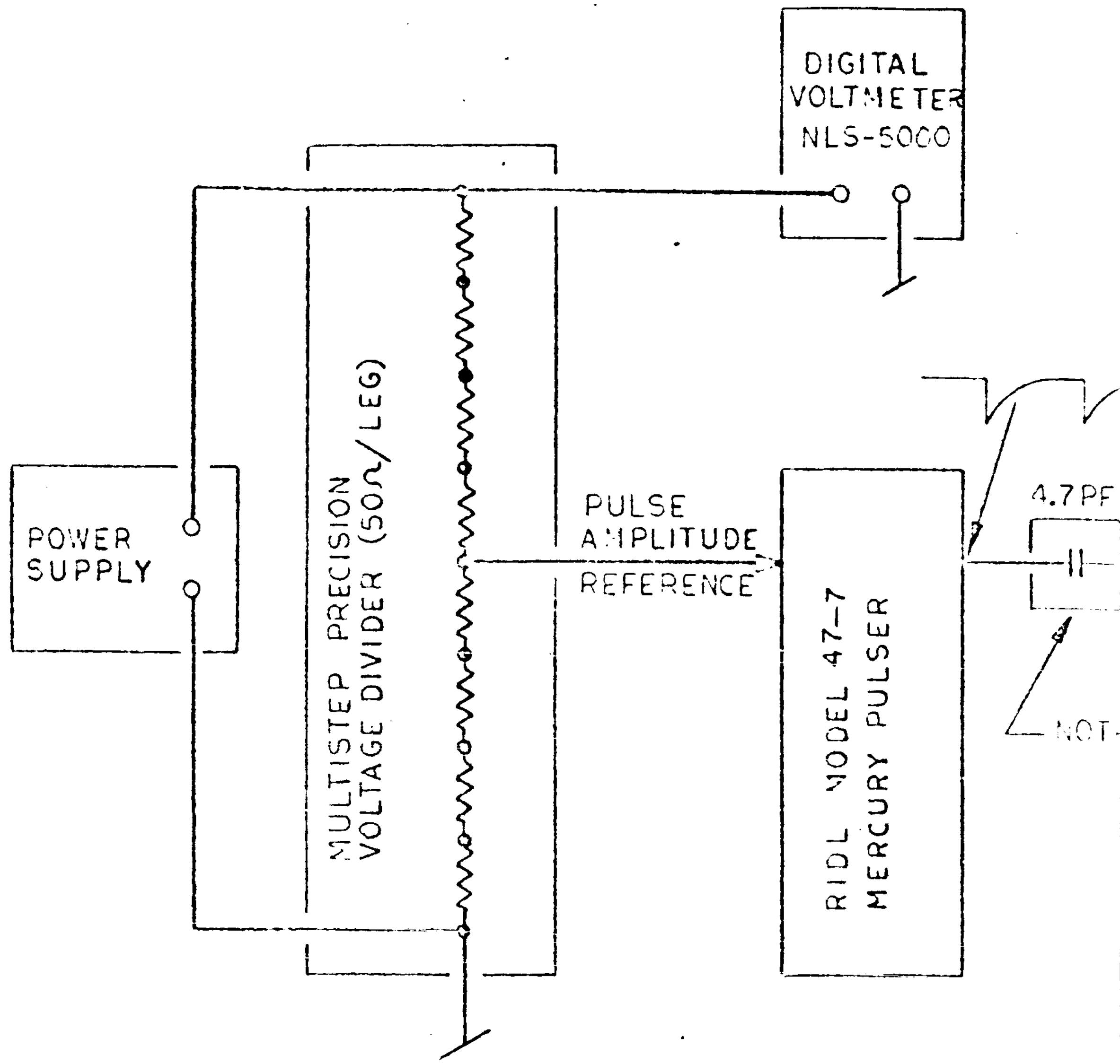
3.3 Gain

This subsection discusses such parameters as linearity, dynamic range, loading performance, susceptibility to supply-voltage variations, and thermal performance. The time allotted to the design and evaluation of this amplifier has not permitted analytical optimization of the amplifier roll-off characteristic for minimum thermally-induced gain variations. Data is presented, however, for the thermal performance of the amplifier shaping characteristic as described in subsection 3.2, and also under conditions of empirical adjustments.

3.3.1 Linearity, Dynamic Range, and Loading

General linearity, noise, and thermal tests were performed with the setup shown in Figure 3.3-1. Use of a calibrated capacitive load box and repetitive input levels for respective loads produced the characteristics listed in Table 3.3-1. Differential linearities for output loadings up to 200 pF and over a 10-V dynamic range were less than 1%, the exact measurements being limited in accuracy by the nonlinearities in the test equipment. Capacitive loading produces gain variations of approximately .15%/100 pF for pulses up to 10 volts and load capacitance up to 300 pF. For a load capacitance of 400 pF, serious rate limiting occurs above 5 volts.

To evaluate the margin of dynamic range available beyond the 10-V design requirement, a 15-V thermal test was performed with 100-pF loading (see Table 3.3-2) producing linearity results at 15 volts comparable to those observed at 10 volts.

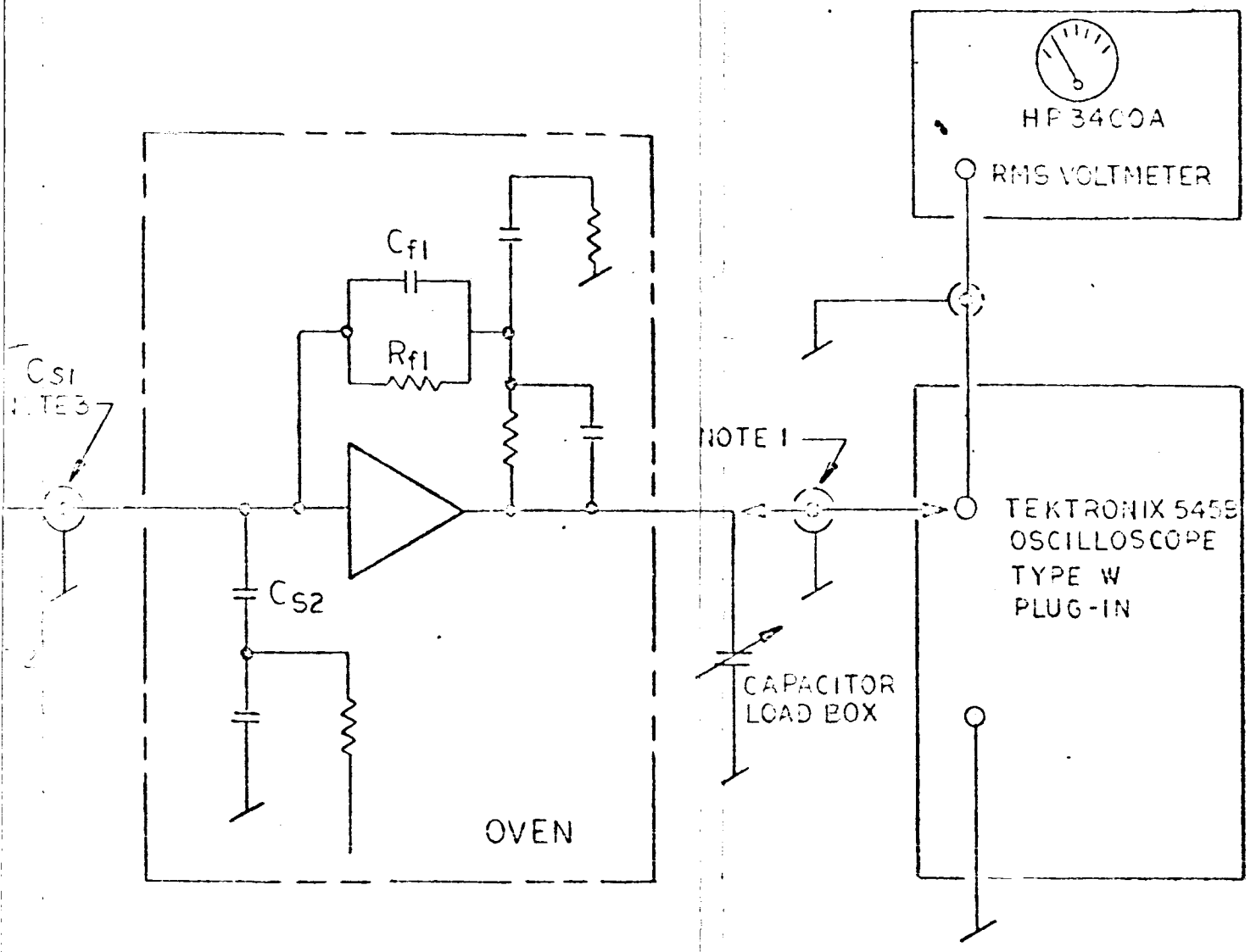


Notes: 1. a) For load test: x 10 probe @10 Meg, 7 pF.

b) For thermal tests: RG58C/U cable, ≤ 100 pF total.

2. Charge reducing network in guarded cylindrical case.

3. During oven testing, RG58C/U cable used and total cable capacitance (C_{s1}) calibrated. Effective simulated detector capacitance = $C_{s1} + C_{s2} = C_D$



TEST SETUP FOR LINEARITY, LOADING, AND THERMAL MEASUREMENTS

FIG. 3.3-1

Peak Amplitude, V				
C_L = 7 pF	C_L = 107 pF	C_L = 207 pF	C_L = 307 pF	C_L = 407 pF
9.960	9.980	10.014	10.021	10.094
7.472	7.485	7.498	7.513	7.539
4.972	4.987	4.983	5.003	5.002
2.482	2.489	2.504	2.510	2.505

Table 3.3-1

Linearity Vs. Load Capacitance

(C_{c4} = 20 pF; R_{c4} = 510 Ω; C_D = 100 pF)

+85°C	+50°C	0°C	-25°C
15.14	15.08	15.19	15.22
12.62	12.58	12.64	12.68
10.09	10.06	10.13	10.13
7.53	7.54	7.57	7.61
5.05	5.06	5.07	5.11
2.59	2.54	2.55	2.57

Table 3.3-2

Dynamic Range Test

(C_{c4} = 20 pF; R_{c4} = 510 Ω; C_L = 100 pF; C_D = 100 pF)

3.3.2 Thermal Performance

To calculate effects of finite and complex values of feedback factor (F) on pulse amplitude, Marshall approximates F using time constants of the same order as the shaping time constants (Appendix, p 20). The resultant pulse peak value (independent of τ_{f1} effects) is then approximately

$$V_{peak} \cong \left(\frac{Q_D}{eC_{f1}}\right)\left(\frac{R_{f2}+R_{f3}}{R_{f3}}\right)\left\{1-\frac{1}{2F_1}\left[1+\frac{\tau_B}{3\tau}\left(1-\frac{4\tau_E}{\tau}\right)\right]\right\} \quad (3.3\text{-}1)$$

where

$$F_1 = F_o\left(\frac{R_{f1}+R_D}{R_D}\right)\left(\frac{R_{f3}}{R_{f2}+R_{f3}}\right)\left(\frac{C_{f1}}{C_A+C_D}\right). \quad (3.3\text{-}2)$$

The last term represents the correction to the closed-loop gain caused by finite feedback factor and bandwidth. This correction depends on transistor parameters and is highly temperature sensitive. Taking into account effects of finite τ_{f1} on peak amplitude, equation (3.3-1) may be rewritten

$$V_{peak} \cong \left(\frac{Q_D}{eC_{f1}}\right)\left(\frac{R_{f2}+R_{f3}}{R_{f3}}\right)\left(1 + E_1 + E_2\right)$$

where E_1 = transistor parameter dependent gain variation

$$= \frac{-1.066}{2F_1}\left[1 + \frac{\tau_B}{3\tau}\left(0.963 - \frac{4.22\ \tau_E}{\tau}\right)\right]$$

E_2 = effects of τ_{f1} on external pulse-shaping (see equation 3.1-2)

$$= -.053$$

Using the amplifier shaping parameters of subsection 3.2 which are as follows:

$$F_o \equiv 10^7$$

$$F_1 \equiv 10^3$$

$$\tau = 1\ \mu s$$

$$\tau_B = 322\ \mu s$$

$$\tau_E = 520\ ns$$

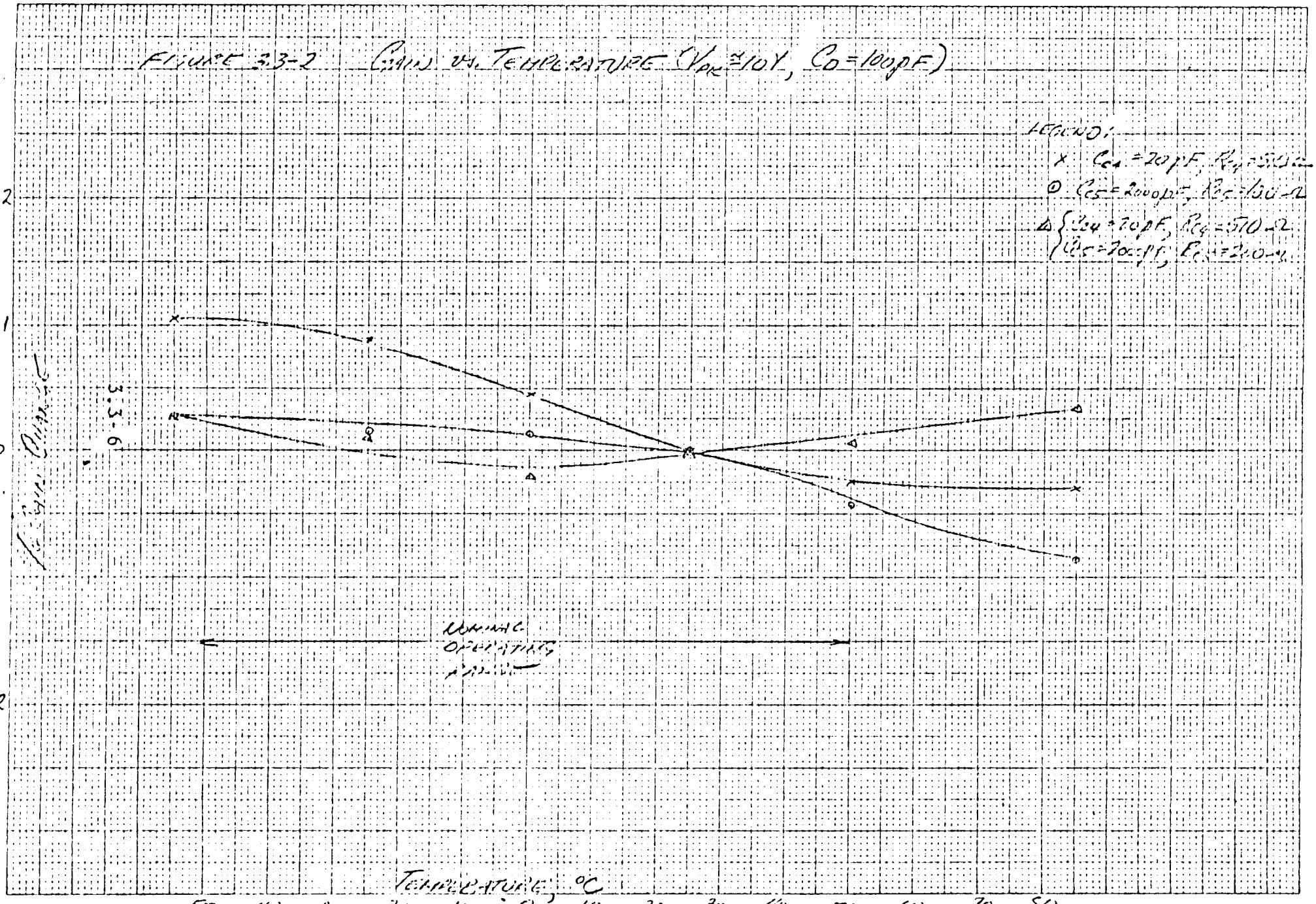
The gain correction factor E_1 is calculated to be +.07. This represents a peaking effect, which is most sensitive to thermally induced gain changes. The term E_2 is calculated using values of precision components and represents a small thermally sensitive error ($\leq$0.1%/100°C).

Results of thermal gain stability tests for C_D = 100 pF are shown in figure 3.3-2. Similar data, though not plotted, have been taken for simulated detector capacitances of 35 pF and 300 pF. Gain stabilities of better than ±0.25% were attainable between ±50°C with experimental adjustment. Adjustment of τ_B and τ_C to smaller values consistent with loop stability requirements should reduce these gain variations.

3.3.3 Supply Voltage Variations

Susceptibility of gain to supply voltage variations is shown in Table 3.3-3. Two significant variations occur and

FIGURE 3.3-2 CHANGE VS. TEMPERATURE (V_{DR}=10V, C_O=100pF)



+18 V		+6 V		-6 V		-12 V	
+20	9.660	+8	9.690	-8	9.680	-14	9.680
+18	9.681	+6	9.680	-6	9.680	-12	9.680
+16	9.725	+4	9.680	-4	9.680	-10	9.725

Table 3.3-3

Gain Vs. Supply Voltage

are as follows:

1) +0.45%/-11% (-18 V)

2) +0.45%/-17% (-12 V)

All other variations are less than 0.2% for the intervals measured. If it becomes desirable to tolerate supply variations as large as the experimental values, further optimization of transistor operating points should be made. This is a relatively simple matter.

3.4 Noise Performance

This subsection compares theoretical and measured values of noise for this charge-sensitive amplifier configuration. Also listed are noise levels as functions of detector capacitance.

3.4.1 Theoretical Levels

For the general case of charge-sensitive amplifiers, the effective amplifier noise, normalized to KeV, rms is given by

$$\overline{E_N^2} = \frac{1}{2\pi\, Q^2\, h_M^2} \left\{ \overline{i_N^2}\, \tau \int_0^\infty \frac{X^{2m-2}\, dX}{(1+X^2)^{n+m}} + \gamma \sqrt{\overline{e_N^2}\ \overline{i_N^2}}\, (C_f + C_s) \int_0^\infty \frac{X^{2m-1}\, dX}{(1+X^2)^{n+m}} + \frac{\overline{e_N^2}\, (C_f + C_s)^2}{\tau} \int_0^\infty \frac{X^{2m}\, dX}{(1+X^2)^{n+m}} \right\} \quad (3.2\text{-}17)$$

(See ref. 3.4-1)

3.4-1 J. H. Marshall, "Pulse Shaping in Pulse-Height Analyzer Systems," ATC Internal Report No. 2, July 1966, p. 67.

where $Q = 4.57 \times 10^{-17}$ C/KeV

and h_M is the maximum value of

$$h(t') = h(t/\tau) = \frac{1}{2\pi j} \oint_C \frac{Z^{m-1} e^{Zt'} dZ}{(1+Z)^{n+m}} \qquad (3.4\text{-}2)$$

and m = number of differentiators = 1

n = number of integrators = 1

γ = 0 (for FET input stages)

The pertinent noise voltage and current are expressed as follows:

$$\overline{e_N^2} \equiv \frac{2.8\ KT}{g_m} \qquad (3.4\text{-}3)$$

$$\overline{i_N^2} = 2q(I_g + I_{LD}) + \frac{4KT}{R_{f1}} . \qquad (3.4\text{-}4)$$

Consider the amplifier alone where

I_{LD} = Detector Leakage Current = 0

$g_m = 2.24 \times 10^{-3}$ (2N4417 @ I_D = 1 mA)

$I_g \doteq 10^{-10}$ A.

Under these conditions

$$\sqrt{\overline{e_N^2}} = 2.24 \times 10^{-9} \text{ V}/\sqrt{\text{Hz}}$$

$$\sqrt{\overline{i_N^2}} = 6 \times 10^{-14} \text{ A}/\sqrt{\text{Hz}}$$

Insertion of all pertinent values into equation (3.4-1) yields

$$\sqrt{\overline{E_N^2}} = 5.04 \text{ KeV, rms} \quad (\tau = 1 \text{ μs}, C_D = 100 \text{ pF})$$

Under the specified conditions, the optimum time constant for $I_{LD} = 0$ is calculated to be 3.94 μs with an associated noise

$$\sqrt{\overline{E_N^2 \text{opt}}} = 3.47 \text{ KeV, rms}$$

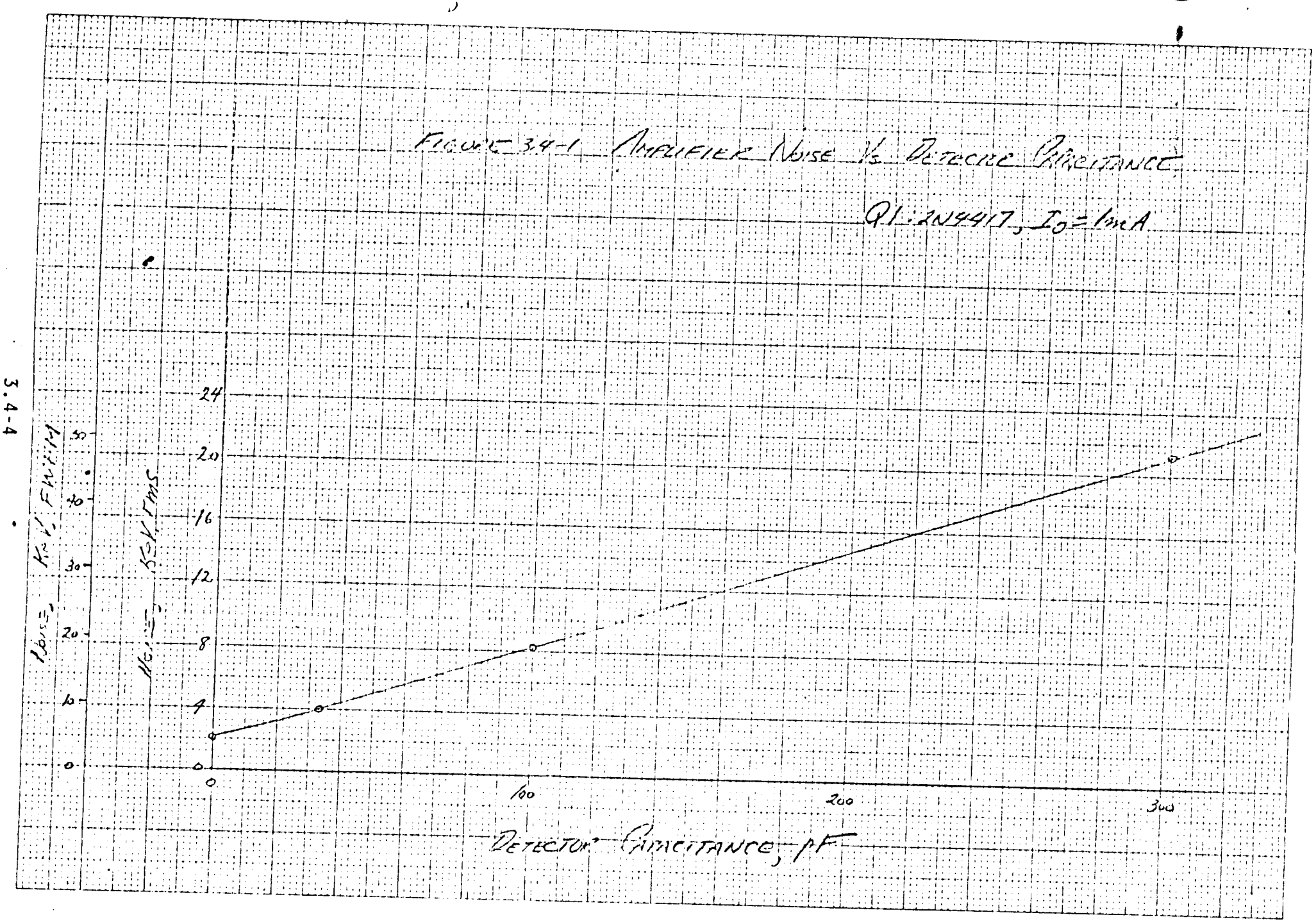
Since voltage noise production as a function of input noise current varies as $\tau^{\frac{1}{2}}$, finite values of detector leakage currents will have lower optimum time constants than 3.94 μs, the actual optimum value being a compromise between the detector and amplifier requirements.

3.4.2 Noise Measurements

Several 2N4417 N-channel FET's were sampled for noise performance by insertion into the Q1 position in the breadboard. All units displayed noise characteristics within 2% of each other at 1 mA drain current. One such unit was used to perform a noise vs. detector capacitance test, the results of which are shown in figure 3.4-1. The 100-pF noise level was measured to be 8.2 KeV, rms, compared with the theoretical value of 5.04 KeV. The measured value is representative of

$$\sqrt{\overline{e_N^2}} = 3.64 \times 10^{-9} \text{ V}/\sqrt{\text{Hz}},$$

neglecting effects of current noise.



3.4.3 Improvement of Noise Performance

Two basic adjustments may be performed to the input stage to improve noise performance. These are

1) Increasing g_m by increasing I_D.

2) Increasing g_m by paralleling FET's.

The drain current characteristic for a FET may be approximated as follows:

$$I_D = I_{DSS}\left(\frac{V_{GS}}{V_P} - 1\right)^2 \qquad (3.4\text{-}5)$$

where I_{DSS} = drain saturation current

V_{GS} = gate-to-source voltage

V_P = pinch-off voltage

The transconductance is therefore

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2}{V_P}\sqrt{I_{DSS}\ I_D} \qquad (3.4\text{-}6)$$

Since voltage noise varies as $g_m^{-\frac{1}{2}}$, it must similarly vary as $I_D^{-\frac{1}{4}}$. As a result, high values of I_{DSS} together with high basic values of g_m are two necessary parameters of low-noise FET's. The 2N4417 has a spread in specified values of I_{DSS} of 5 to 15 mA. One unit used in several noise tests had an

I_{DSS} = 7.5 mA. The theoretical improvement in noise voltage at 7.5 mA over that obtained at 1 mA is $8^{\frac{1}{4}} = 1.65$. The measured aggregate improvement was 1.27.

Paralleling n identical transistors that share load current equally, on the other hand, increases g_m n-fold. If the net load current is increased n times, so that each FET carries the same initial current as the single stage of the previous example, the voltage noise component is decreased by $n^{\frac{1}{2}}$. Therefore, increased operating currents and use of paralleled input stages will notably enhance noise performance beyond those levels described in this report.

A manufacturer's sample of a new experimental low-noise FET (FN641) became available during the preparation of this report. While only one sample was available, and reproduction parameters from one unit to the next could not be verified, the following data is of interest:

$I_{DSS} > 40$ mA

$g_m \cong 15 \times 10^{-3}$ mho @ 40 mA

Amplifier noise = 7 KeV, rms @ 1 mA

P_D = No data available (very hot at 20 mA and 6 V).

Units such as this produce short-term values of I_{DSS} far in excess of its average power handling capability. While not yet thoroughly tested, transistors such as this promise even better solutions to the perennial problem of low-noise amplification.

4.0 SUMMARY

Some noteworthy differences between the amplifier described in this report and its conjugate predecessor (described in the appendix) are as follows:

1) Dynamic range has been increased.

2) The amplifier is configured to accept low-noise N-channel FET's at the input compared to P-channel units for the design in the appendix.

Pulse amplitudes of 10 V at cable loadings of 300 pF, and amplitudes of 15 V at loadings of 100 pF may be stably handled with this amplifier. Noise performance is improved approximately 40% over that obtained with its conjugate counterpart at the same operating point. The 2N4417 FET's used in these evaluations displayed uniformly lower noise characteristics from unit to unit than the P-channel units (specially selected in 1964) to which they were compared. It appears feasible that still new reductions in amplifier noise may be accomplished through the use of optimization techniques described in 3.4.3.

Appendix

An Amplifier and Discriminator for use with Solid State Radiation Detectors in Spacecraft Applications

Jet Propulsion Laboratory
Unpublished Internal Report
February, 1964

AN AMPLIFIER AND DISCRIMINATOR FOR USE WITH SOLID STATE RADIATION DETECTORS IN SPACECRAFT APPLICATIONS

J. Howard Marshall
Jet Propulsion Laboratory
California Institute of Technology
February 24, 1964

TABLE OF CONTENTS

TABLES

LIST OF FIGURES

I. INTRODUCTION

Because of their small size, rugged construction, and negligible power consumption, solid state detectors for ionizing particles have been proposed for several coming interplanetary experiments. For example, the Mariner C Cosmic-Ray Telescope will use such detectors to measure part of the energy spectrum of interplanetary cosmic-ray protons and alpha particles. Also using solid state detectors, the Surveyor Alpha Scattering Experiment measures the energy of back-scattered alpha particles from the lunar surface in order to determine its composition. A similar scheme has been proposed[1] for a measurement of the composition of the Martian atmosphere.

The general usefulness of these detectors motivated the development of the amplifier and discriminator described below, which are intended to be part of an instrumentation system applicable to many space experiments. Several similar circuits already exist but were built using a design approach which differs fundamentally from the one used here. After these differences are outlined, the amplifier and discriminator will be described in detail. Future reports will contain additions to this instrumentation system as they are developed.

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(1) E. Franzgrote and J. H. Marshall, "Analysis of the Martian Atmosphere by Alpha Particle Bombardment - The Rutherford Experiment", JPL Inter-office Technical Memorandum, November 1963.

II. DESIGN APPROACH

Past designs of amplifiers and discriminators often resulted in gains, thresholds, and pulse shapes depending strongly on semiconductor parameters. The circuits were almost entirely empirically produced, because the wide variations in these parameters made accurate theoretical predictions most difficult. Since an optimum design could result only by rather improbable accident, power was wasted, and many components were present which added only to the number of parts which might fail. Furthermore, sensistors or other temperature variable elements were used to compensate for thermally-induced semiconductor changes. This compensation, which could only be achieved by time-consuming selection of sensistors and semiconductors, resulted in poor reproducibility of circuit performance and was effective only over a very limited temperature range. Sometimes sufficiently stable operation could only be achieved by matching the drifts of one circuit to drifts of the opposite sign in a subsequent circuit. This arrangement limited the versatility of the design because circuits of the same function ceased to be interchangeable.

Virtually no provision was made for non-thermally induced semiconductor variations. The temperature compensating schemes were particularly questionable in this regard because they required that second order effects, such as transistor temperature coefficients, remain stable over long periods of time. The neglect of aging in circuits which had to operate several years without repair or adjustments dangerously compromised reliability.

Finally, even with temperature compensation, experiments requiring total gain and threshold stabilities better than about 5% had to rely heavily on calibration data, providing another avenue for possible failure.

In that reliability, which obviously includes drifts not exceeding tolerance, is a prime consideration in the design of the amplifier and discriminator described below, large amounts of feedback are used so that the transistor dependent parts of gains and thresholds are of the same order as the tolerable drifts (typically 1%). Then

even large semiconductor variations perturb the gain and threshold by a tolerable amount. In addition, theoretical analysis is used to optimize the design, resulting in each circuit containing inherent stability and reliability but not using excessive weight and power. As in any carefully executed scientific approach, theoretical predictions are checked experimentally, and an effort is made to understand any discrepancies present. Only when there is approximate agreement between theory and experiment can confidence be gained that a particular circuit measurement is not a special case difficult to reproduce.

Because temperatures are difficult to predict and control in space, the operating temperature range for these circuits is made as large as practical, and extends from +50°C to -50°C. The upper limit results from the intolerable noise and reduced reliability of solid state detectors operating over +50°C, while the lower limit is given by the rapid decrease of transistor current gains below -50°.

Because the variations of transistor parameters over a 100°C temperature range exceed all but the most unlikely variations caused by the aging of premium transistors during several years, stable operation during such a temperature change implies stable operation during the life of an experiment. For example, transistor current gains at -50°C are less than half their value at +50°C, while the probability of a factor of 2 decrease in gain from aging is of the same order as total catastrophic failure, which hopefully is negligibly small. Obviously, if elaborate temperature compensation were provided, then the non-thermally induced drifts would be considerably greater than the thermal drifts, and this method for estimating the effect of aging would no longer be valid.

Finally, because these circuits are sufficiently stable for most conceivable environmental conditions, calibration may be used only as an additional hedge against the unexpected, rather than as an essential part of the operation of an experiment.

III. AMPLIFIER

3.1 General Theory of Operation

A simplified schematic diagram of the amplifier is shown in Figure 1, where a capacitive current source represents the solid-state detector, for which bulk resistance and leakage have been neglected. Although about 20 ns are required for most of the detector charge to be collected, the detector response is approximated by a delta-function, because the collection time is short compared to the amplifier response time.

The charge Q_D produced by the detector is proportional to the energy loss E of a charged particle passing into the detector depletion layer and is given by:

$$Q_D = q \frac{E}{E_o} \qquad (1)$$

where: q = charge on the electron = 1.6×10^{-19}C

E_o = energy loss per hole-electron pair = 3.5 eV in Silicon

The energy loss per hole-electron pair is predicted by one detector manufacturer * to be stable to about ± 1% from -50°C to +50°C. So long as the particles stop within the depletion layer, the detector charge output should also be stable to about ± 1% and independent of detector bias voltage. Because the detector capacity C_D depends on the bias voltage, which may not be particularly stable, the amplifier is designed to have an effective input capacity much larger than the detector capacity. Then most of the detector charge is deposited on the feedback capacitor C_{f1}, and the output voltage becomes nearly independent of the detector capacity and transistor parameters, making this circuit truly a charge sensitive amplifier.

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* Solid State Radiations, Inc., Los Angeles, California

In order to avoid the weight, power and drifts involved in the usual method of using two amplifiers in series to provide sufficient gain, this amplifier is designed to have a conversion gain of 1V/M eV. If this conversion gain were obtained with the feedback capacitor connected directly between the amplifier output and input, the resulting capacitance of 0.05 pF would be strongly dependent on stray capacity and not very stable. Placing an attenuator (Z_{f2} and Z_{f3}) between the feedback capacitor and the output allows a practical value of capacitance (5 pF) to be used, together with providing a convenient place for pulse shaping. The output voltage is then approximately related to the energy loss by:

$$\frac{V_{out}}{E} = \frac{q}{E_o C_{f1}} \left(\frac{Z_{f2}}{Z_{f3}} \right) = \frac{qR_{f2}}{E_o C_{f1} R_{f3}} \frac{p\tau_{f3}}{(1 + p\tau_{f2})(1 + p\tau_{f3})} \qquad (2)$$

where: τ_{f2} = rise time constant = $R_{f2} C_{f2}$

τ_{f3} = decay time constant = $R_{f3} C_{f3}$

p = Laptace transform variable

$Z_{f3} << Z_{f2}$ $\qquad$ $M_o \longrightarrow \infty$

$Z_{f3} << Z_{f1}$ $\qquad$ $R_{f1} \longrightarrow \infty$

In order to obtain the optimum signal-to-noise ratio[2] and a pulse slowly varying near the peak, the rise time constant is made equal to the decay time constant, producing the pulse shown in Figure 2. In this case, the output voltage as a function of time is approximately:

$$\frac{V_{out}}{E} = eM_c \left(\frac{t}{\tau} \right) \text{Exp} \left(- \frac{t}{\tau} \right) \qquad (3)$$

---

(2) E. Fainstein, "Considerations in the Design of Pulse Amplifiers for Use with Solid State Radiation Detectors", Tennelec Instrment Co., Oak Ridge, Tennessee.

where: τ = shaping time constant = $\tau_{f2} = \tau_{f3}$

M_c = conversion gain = $\frac{\text{Pulse peak voltage}}{\text{Particle energy loss}}$

$$M_c = \frac{qR_{f2}}{eE_o C_{f1} R_{f3}}$$

e = 2.72 = base of natural logarithms

Because the pulse shaping is done within the amplifier rather than later, no additional amplifier dynamic range is required as a result of the pulse shaping, although equal rise and fall time constants reduce the conversion gain by a factor of 1/e.

The value for the shaping time constant is a compromise between maximum tolerable counting rates, NOISE, and amplifier bandwidth, and can be varied to suit a particular experiment. The amplifier described in detail here used a 2 μs shaping time constant. A version with a 0.5 μs shaping time constant and a conversion gain of 0.5 V/MeV was also found to operate satisfactorily, although final optimization on such a circuit has not been performed.

Finite R_{f1} causes a 15% undershoot of the pulse for τ = 2 μs and $R_{f1} C_{f1}$ = 25 μs. The area of this undershoot equals the area of the positive part of the pulse because detector current does not flow continuously. Therefore, for linear circuits, no net charge is transferred to any coupling capacitors. The base-line will have recovered to 0.25% of the pulse peak voltage after 100 μs, permitting counting rates as high as 10 Kc/s with less than 1% pile-up of the pulse tails.

3.2 Circuit Details

Because the amplifier open loop gain and bandwidth are finite, some charge flows onto the detector capacity and onto the amplifier input capacity. Because this charge loss depends upon unstable transistor parameters and detector capacity, the amplifier gain and bandwidth must be made as large as possible without resorting to complex circuits or to large power consumption. Two versions of the basic amplifier configuration (see Fig. 3) were developed. One is intended for spacecraft applications, while the other is for ground based laboratory use. The latter compromises reliability for ease in selecting components and for versatility in operating with any detector capacity without circuit changes. In the spacecraft version, the amplifier is optimized to the capacity of the detector with which it is being operated, and the transistors are stringently selected to provide a large allowance for deterioration caused by aging.

The basic configuration consists of a grounded source field-effect transistor input stage, two grounded emitter stages, and an emitter follower output stage. Negative feedback with pulse shaping as described in the previous section is applied from the output back to the input. In order to make the DC gate voltage of the input transistor independent of the detector bias voltage, the detector is capacitively coupled to the amplifier. The size of this capacitor (C_1) can be reduced a factor of ten without increasing the drifts if the feedback capacitor is returned directly to the detector instead of to the gate of the field-effect transistor. A small capacitor reduces the physical size of the amplifier and decreases the sensitivity to low frequency detector noise.

A field effect transistor was chosen for the input stage (Q1) because of its low noise and high input impedance. Because the noise of a field-effect transistor is nearly independent of its standing current, the transistor can be operated with a sufficiently large drain current to produce a transconductance over 1500μmho. The gate current, which is usually much smaller than detector leakage current, adds negligibly to the noise and to bias instabilities even at high impedance levels. The added complexity of the usual cascode configur-

ation for the input stage was found not to be justified by reduced noise.

The 2N2497 and 2N2500 field-effect transistors were chosen because of their low noise figure, high transconductance and small capacity, and because they would operate at 1mA of drain current required for obtaining optimum gain and bandwidth. If the drain current at zero gate-source voltage does not exceed the current in R_1, then the second stage will be cut off, resulting in amplifier failure. At 100°C the maximum drain current is 70% of its room temperature value, and thus the room temperature maximum drain current should exceed 1.3mA. In the laboratory version, this current is selected to exceed 1.5mA, while for spacecraft application an additional margin is left by selecting for 2mA or greater.

Most of the voltage gain is provided by the second and third stages (Q2 and Q3), both of which are in the same TO-18 can. Because of the large voltage gain, the bandwidth is determined primarily by the collector-base capacity. The principal advantages of the 2N2973 transistors are their high current gain (typically 450) and their low collector-base capacity (3.3 pF). Secondary advantages are a large collector output impedance and low noise figure. Their current gain-bandwidth product of 80 Mc/s is adequate. For the spacecraft version, the transistors are selected to have current gains that equal or exceed the typical value.

An emitter-follower output stage (Q4) provides a low output impedance, so that difficulties with non-linearities and gain drifts associated with a separate buffer outside the feedback loop are minimized without large standing currents. The transistor for this stage must have a high gain-bandwidth product so as to prevent ringing for capacitive loads, while also having a sufficiently large current gain to produce a low output resistance. The 2N709 has a gain-bandwidth product of 800 Mc/s with a minimum current gain of 50. For the spacecraft amplifier, this transistor is selected to have a current gain in excess of 100 so that loads as small as 1K do not appreciably increase the gain drifts.

In the laboratory version, a 46.7 ohm resistor is placed in series with the output, so that reflections from a 50 ohm cable on the output will be reduced. For spacecraft applications, the amplifier probably would be connected directly with short wires to the subsequent circuits.

In order to increase the voltage gain of the third stage without increasing power consumption, the load resistor for the third stage is boot-strapped to the emitter-follower output. This configuration also provides nearly constant base drive to the output stage, resulting in improved linearity and less problem with rate limiting caused by the capacity on the collector of Q3. The resistor values are chosen so that the effective resistance of the 9.01K resistor is increased to 36.4K. The 4.32K resistor between the output and the 9.01K resistors reduces the effective resistance but also eliminates a strong dependence on the unpredictable collector output impedance of Q3 or on load resistance. Besides, further increases in this effective resistance do not appreciably reduce drifts because bandwidth effects, which are independent of this resistance, now dominate.

The transistor operating points are fixed by the same feedback loop which determines the AC gain, reducing complexity by eliminating coupling and bypass capacitors. The choice of operating points is a compromise between gain, bandwidth, load dependence, noise, and power consumption. It can be shown that maximum gain is obtained when the source resistance for the second and third stages equals their transistor base input resistance. If this condition is imposed, then the current in the third stage and the collector voltages remain the only free variables. The collector voltages were chosen to be about 4V to 5V because the collector-base capacity increases rapidly for smaller voltages. The field effect transistor has a drain voltage of -5.3V, which operates the transistor in the pinch-off region with a low gate-drain capacity. Fast response and small load dependence indicate that the current in the third stage, and thus all the transistor currents, be as large as possible. Low noise, low power consumption, and field-effect transistor limitations require small

currents. The values shown in Figure 3 represent a compromise between these conflicting requirements.

The maximum output voltage is determined by the point at which Q_4 saturates. If the field-effect transistor leakage current is neglected, the voltage on the emitter of Q_4 is given by:

$$V_{e4} = V_{gs} + \left(\frac{V_{gs} + 17.9V}{R_B}\right) R_{f1}$$

where: V_{gs} = gate-source voltage of Q_1

and the resistors are as shown in Figure 3.

The collector voltage is then related to the emitter voltage by:

$$V_{c4} = 11.8V - \frac{R_{c4}}{R_{e4}} V_{e4}$$

and the maximum output voltage is:

$$V_{max} = V_{c4} - V_{e4} - V_{sat} \qquad (6)$$

$$= 11.8V - \left(\frac{R_{c4} + R_{e4}}{R_{e4}}\right)\left[V_{gs} + \frac{V_{gs} + 17.9V}{R_B} R_{f1}\right] - V_{sat}$$

where: V_{sat} = saturation voltage of Q_4 = 0.2V to 0.5V for load resistances between infinity and 1K.

If the power supply voltages remain constant, the principal sources of drift in V_{e4} and V_{max} are variations in R_B and V_{gs}. Although V_{gs} may vary as much as 0.5V between different transistors, it remains stable to about 0.1V over the temperature range. For critical applications R_B is matched to the particular field-effect transistor being used, so that V_{e4} equals its optimum value of 3.4V. If R_B were a composition carbon resistor, which may have a

temperature coefficient as large as 1,500 ppM/°C, V_{e_4} could drift from this cause alone by ± 0.25V, resulting in a drift of the maximum output voltage by ± 0.4V. In applications where stability of the amplifier dynamic range is important, a carbon film resistor, which is physically large but has a temperature coefficient less than 500 ppM/°C, reduces this drift to ± 0.1V. Experimentally, the maximum output voltage is found to remain stable to 0.15V for temperatures between -50°C and +50°C.

The maximum output voltage is limited by the available supply voltage and by the current gain and collector breakdown voltage of Q_4. For spacecraft applications, the maximum output voltage should not exceed 5V for 1K loads or 7V for 2K or higher loads. As shown by equation (6), the dynamic range can be reduced by increasing R_{c_4}.

The laboratory amplifier is adjusted for a maximum output voltage of about 7V, and its linearity and gain are shown in Figure 4. The variation of the instantaneous conversion gain over the entire dynamic range is less than 0.5%. This variation includes non-linearities in a precision mercury pulser * and in the discriminator (see section 4).

A photograph of an amplifier constructed for laboratory use is shown in Figure 5. Because capacitive coupling of the output signal to the input reduces the gain, the input stage is isolated from the remainder of the amplifier by a metal shield. Since any pickup of externally generated signals increases the noise, the amplifier is enclosed in a metal box, and the power supplies are decoupled with 1 ms time constants. If possible, the detector should be connected directly to the amplifier in order to avoid the noise and capacity produced by an input cable.

Because improper coupling of ground currents can lead to ringing and gain

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* RIDL Model 47-7

drifts, common ground points, represented by circled numbers in Figure 3, are used to isolate one stage from another. The metal shield provides a low impedance return for interstage and feedback ground currents.

Capacitive coupling of the base of Q_2 to the collector of Q_3 constitutes positive feedback. In order to avoid the resultant ringing and oscillation, the base lead of Q_2 on the output side of the shield is kept as short as possible, and the case of Q_2 and Q_3 is grounded. Also, the components in the collector circuit of Q_3 and those associated with Q_4 are kept physically removed from the base of Q_2. With the above precautions, the effects of pick-up, stray capacity and ground currents become unobservable.

The amplifier is protected against damage from power supply transients by the 100 ohm series decoupling resistors, which limit the current, and by diodes, which prevent breakdown of the relatively delicate emitter-base junctions. The diode on Q_4 also allows current from Q_3 to pull capacitive loads negative, so that even for loads greater than 200 pF, the output pulse shape remains constant.

3.3 Stability against Oscillation

Because more than two poles are within the feedback loop, oscillation, which would render the amplifier useless, is possible. Because a low gain drift and a large margin of safety against oscillation are competing requirements, an optimum design necessitates accurate prediction of oscillatory conditions. These conditions depend on the amplitude and phase of the complex feedback factor, the calculation of which is based on the simplified schematic of Figure 6 and on the approximate equivalent circuits of Figure 7. For this calculation the loop is considered opened at the point marked X in Figure 6, and the feedback factor is defined as the output voltage for unit voltage applied to the input side of the indicated point. Poles and zeroes with angular frequencies in excess of 10^9 radians per second are neglected because they are over an order of magnitude removed from the frequency at gain cross-over ($|F| = 1$). The collector-base resistance (r_c in Figure 7) is also neglected because the times of interest are short compared to $r_c C_{ob}$ (typically 66μs). For longer times r_c reduces the gain by about a factor of two.

With the above approximations the complex feedback factor can be written as (see Figure 6):

$$F = F_o \left\{ \frac{-(1+j\omega\tau_{f1})(1+j\omega\tau)^2(1+j\omega\tau_{c1})(1+j\omega\tau_{c2})(1+j\omega\tau_{c3})(1-j\omega\tau_J)}{(1+j\omega\tau_A)(1+j\omega\tau_B)(1+j\omega\tau_C)(1+j\omega\tau_D)(1+j\omega\tau_E)(1+j\omega\tau_F)(1+j\omega\tau_G)(1+j\omega\tau_H)(1+j\omega\tau_I)(1+j\omega\tau_K)} \right\} \quad (7)$$

where: $j = \sqrt{-1}$

ω = angular frequency

F_o is the feedback factor for DC and is given by:

$$F_o = \frac{M_{v1}\ M_{v2}\ M_{v3}\ M_{v4}\ R_D}{R_{f1} + R_D} \quad (8)$$

where: M_{v1} = voltage gain of $Q_1 = g_m R_{L1}$

M_{v2} = voltage gain of $Q_2 = \dfrac{R_{L2}}{r_{e3}}$

M_{v3} = voltage gain of $Q_3 = \dfrac{R_{L3}}{r_{e3}}$

M_{v4} = voltage gain of $Q_4 = \dfrac{R_L}{R_L + r_{e4}}$

R_{L1} = load resistance of $Q_1 = \dfrac{R_1\ \beta_2\ r_{e2}}{R_1 + \beta_2\ r_{e2}} \parallel h_{fb}$

R_{L2} = load resistance of $Q_2 = \dfrac{R_2\ \beta_3\ r_{e3}}{R_2 + \beta_3\ r_{e3}}$

R_{L3} = load resistance of $Q_2 = \dfrac{\left(\dfrac{R_3 + 2R_4}{R_4}\right) R_3\ \beta_4\ R_L}{\left(\dfrac{R_3 + 2R_4}{R_4}\right) R_3 + \beta_4\ R_L}$

The following poles and zeros are determined by the pulse shaping networks, and remain stable over the temperature range to about 2%.

$$\tau_{f1} = R_{f1}\, C_{f1}$$

$$\tau = R_{f2}\, C_{f2} = R_{f3}\, C_{f3}$$

$$\tau_D = R_{f3}\, (C_{f1} + C_{f2}) \qquad (9)$$

$$\tau_K = (R_{f2} + R_{f3})\, C_{f3}$$

The high frequency compensation networks, which are used to prevent oscillation, result in the zeros shown below. The values of these zeros depend only on fixed resistors and capacitors, which do not vary over the temperature range by more than about 1%.

$$\tau_{c1} = R_{c1}\, C_{c1}$$

$$\tau_{c2} = R_{c2}\, C_{c2} \qquad (10)$$

$$\tau_{c3} = R_{c3}\, C_D$$

The large poles given below are produced by transistor dependent capacities and by additional capacity added to control the feedback factor at high frequencies. These poles dominate the response for angular frequencies less than 10^7 rad/sec., and combined with τ_{f1}, τ, and τ_K produce 90° of phase shift at gain cross-over.

$$\tau_A = (C_A + C_D)\left(\frac{R_{f1}\, R_D}{R_{f1} + R_D}\right) \qquad (11)$$

$$\tau_B = \frac{(C_B + C_D)(\tau_2 + \tau_3) + M_{v1}\, C_{gd}\, \tau_1}{C_A + C_D}$$

$$\tau_C = \frac{\tau_3 + \dfrac{\tau_5\, \tau_1}{\tau_2 + \tau_3}}{1 + \dfrac{M_{v1}\, C_{gd}\, \tau_1}{(C_B + C_D)(\tau_2 + \tau_3)}}$$

where:

$$C_A = (1 + M_{v1})\, C_{gd} + C_f + C_{gs}$$

$$C_B = C_{gs} + C_f + C_{gd}$$

$$\tau_1 = R_{L2}\,(M_{v3}\, C_{ob3} + C_{e3})$$

$$\tau_2 + \tau_3 = \tau_1 + R_{L1}\,(M_{v2}\, C_{ob2} + C_{e2})$$

$$\tau_3 = \frac{R_{L1}\left[\tau_1\,(C_{e2} + C_{ob2} + C_{gd}) + \tau_4\, M_{v2}\, C_{ob2}\right]}{\tau_2 + \tau_3}$$

$$\tau_4 = R_{L3}\left[C_{ob3} + C_{ob4} + \frac{C_L + C_{c2}}{\beta_4} + \frac{\tau_{T4}}{R_L}\right]$$

$$\tau_5 = (R_{L1} + R_{c1})\, C_{c1}$$

Additional phase shift near gain cross-over is determined by poles and zeros with time constants of the order of 10ns. The poles and zeros arising from the output emitter-follower and from high frequency roots remaining after factoring out τ_A, τ_B, and τ_C are given below.

$$\tau_E + \tau_F = C_{c2}\left(R_{c2} + \frac{r_{e4}\, R_L}{R_L + r_{e4}}\right) + \frac{C_L\, R_L\, r_{e4}}{R_L + r_{e4}} \qquad (12)$$

$$\tau_F = \left(\frac{R_{c2}\, r_{e4}\, R_L\, C_{c2}}{R_L + r_{e4}}\right)\left(\frac{C_{e4} + C_L}{\tau_E + \tau_F}\right)$$

$$\tau_G = \frac{B + \sqrt{B^2 - 4A}}{2}$$

$$\tau_H = \frac{B - \sqrt{B^2 - 4A}}{2}$$

$$\tau_I = C_D R_{c3} \left(\frac{C_B}{C_B + C_D} \right)$$

$$\tau_J = \frac{C_{gd}}{g_m}$$

where:

$$A = \frac{\tau_{c1} \tau_6^2 \tau_7}{\tau_3 (\tau_2 + \tau_3) + \tau_1 \tau_5}$$

$$B = \frac{\tau_{c1} \tau_3 (\tau_2 + \tau_3) + \tau_6^2 (\tau_5 + \tau_7)}{\tau_3 (\tau_2 + \tau_3) + \tau_1 \tau_5}$$

$$\tau_6^2 = \tau_4 R_{L2} C_{e2}$$

$$\tau_7 = R_{L1} (C_{e2} + C_{ob2} + C_{gd})$$

Typical values for these quantities at +50°C, +25°C, and -50°C are shown in Table 1. The asymptotic approximation of the absolute value of the complex feedback factor for two typical cases is shown in Figure 8.

Oscillation is possible if 180° of phase shift occurs at frequencies less than that frequency for which the absolute value of the feedback factor equals one. This amplitude and phase can be controlled by varying the high frequency compensation elements. In the spacecraft version the compensation is optimized to the specific detector being used, so that the gain drifts will be reduced as much as possible. In the laboratory version, the compensation is relatively fixed, providing ease of use with most detectors but sacrificing gain stability and margin against oscillation.

The phase shift at gain cross-over is critically dependent on the detector capacity. In order to prevent oscillation for detector capacities less than 130 pF, the high frequency feedback factor must be deliberately reduced in amplitude. Although this reduction could be accomplished by adding a capacitor in parallel with the detector, such artificially increased detector capacity would result in unnecessarily increased amplifier noise.

Instead, the high frequency gain of the first stage is decreased by adding a compensating network (R_{c1} and C_{c1}) to the drain of Q_1. Not only does this network decrese the high frequency gain, but it also produces a zero (τ_{c1}) near gain cross-over, resulting in improved phase margin.

Another such zero (τ_{c3}) is provided by a resistor (R_{c3}) in series with the detector capacity. For detector capacities 50 pF or greater, R_{c3} is chosen so that τ_{c3} is fixed at 10 ns. Because a pole (τ_I) tends to cancel the beneficial effect of τ_{c3} for detector capacities much below 50 pF and because the noise from resistors larger than about 200 ohms becomes significant, R_{c3} is fixed at 200 ohms for detector capacities below 50 pF. The detector bulk resistance also adds to R_{c3}, improving the stability of the amplifier.

The value of C_{c1} is then determined by requiring an adequate gain margin under the worst conditions. Calculation shows that the gain margin at -50°C can be up to a factor of two less than at +50°C. Therefore, C_{c1} is chosen so that the feedback factor for a phase shift of 180° at +50°C is 0.25, leaving an additional factor of two at -50°C for transistor variations. Figure 9 shows the resulting values of C_{c1}, R_{c1}, and R_{c3} versus detector capacity.

In the laboratory amplifier, R_{c3} is fixed at 100 Ω, and C_{c1}, which can be removed by a switch, has a value of 200 pF. This compensation provides only marginal stability at -50°C for detector capacities less than 25 pF, but even for zero detector capacity oscillation does not occur at room temperature. Reduced gain drift will result if the compensation is switched out for detector capacities exceeding about 70 pF. However, oscillation may occur for detector capacities less than about 50 pF unless the compensation is switched in.

The output compensation, consisting of R_{c2} and C_{c2} (see Figure 6) reduces the sensitivity of the circuit to capacitive loads. Without this compensation, such loads would produce a pole in the complex feedback factor with a time constant of 10 ns. The output compensation places a pole and a zero (τ_E and τ_{c2}), whose value is relatively independent of load capacity, at time constants of 60 ns and 30 ns

respectively. These time constants reduce the amplitude of the feedback factor near gain cross-over without adding appreciably to the phase shift or to the gain drifts. A third pole (τ_F) proportional to the load capacity has a time constant 4 ns or less for load capacities as large as 200 pF.

An additional effect of load capacity is the introduction of a frequency dependent input capacity to the emitter-follower (Q_4). The use of a fast transistor and of output compensation reduces this effect to a 10% correction in the feedback factor.

Because the prediction of the condition for oscillation is critical in the choice of the compensating elements, the amplitude and phase predicted by equation (7) were checked experimentally. Because frequencies over 10 Mc/s are involved, a direct measurement of the feedback factor versus frequency was not practical. However, for a fixed compensation scheme, the minimum value of the detector capacity to prevent oscillation could both be predicted and measured. A comparison of these values is shown in Figure 10, which provides confidence that equation (7) really predicts amplifier performance.

3.4 Gain Drifts

In order to make use of the inherent ± 1% stability of solid state detectors, the amplifier gain drift should not exceed ± 1%. Because many factors may cause gain shifts of the order of 1% over a 100° C temperature range, an analytical approach is first used to estimate the sensitivity of the gain to various drift producing factors. Proper choice of components for the critical gain determining [illegible] elements can then be made, and assurance can be obtained that the gain does not depend critically on transistor parameters. Approximate agreement between theoretical predictions and experimental results provides confidance that the measurements are correct and not a special case. Also, it is far easier to extrapolate analytically than to measure all conceivable cases.

The closed-loop gain can be written as:

$$A_{cl} = \frac{p\,\tau_K\,(1 + p\,\tau_D)\,R_{f1}}{(1 + p\,\tau)^2(1 + p\,\tau_{f1})}\left(\frac{F}{1 - F}\right) \tag{13}$$

where F is given by equation (7). Because the gain depends mostly on time constants of the same order as the shaping time constant, the closed-loop gain can be approximated by:

$$A_{cl} \cong \left(\frac{R_{f2} + R_{f3}}{p\,C_{f1}\,R_{f3}}\right)\left(\frac{p\,\tau}{(1 + p\,\tau)^2}\right)\left(\frac{F}{1 - F}\right) \tag{13a}$$

for: $\tau_{f1} >> t >> \tau_D$

t = time from the injection of the detector charge.

and: $$F \cong F_o\,\frac{(R_{f1} + R_D)\,C_{f1}\,R_{f1}\,(1 + p\,\tau)^2}{(C_A + C_D)\,R_{f1}\,R_D\,(1 + p\,\tau_B)(1 + p\,\tau_c)\,p\,(R_{f2} + R_{f3})\,C_{f3}}$$

The expression for the feedback factor can be simplified to:

$$F \cong - F_1 \frac{(1 + p\tau)^2}{p\tau(1 + p\tau_B)(1 + p\tau_C)} \qquad (13b)$$

$$F_1 = F_o \left(\frac{R_{f1} + R_D}{R_D}\right) \left(\frac{R_{f3}}{R_{f2} + R_{f3}}\right) \left(\frac{C_{f1}}{C_A + C_D}\right)$$

and the remaining quantities are given by equations (8) to (11).

Substituting equation (13b) into equation (13a), the closed-loop gain is given by:

$$A_{cL} = \left\{\frac{R_{f2} + R_{f3}}{p\, C_{f1}\, R_{f3}}\right\} \left\{\frac{p\tau}{1 + p\left[2\tau + \frac{\tau}{F_1}\right] + p^2\left[\tau^2 + \frac{\tau(\tau_B + \tau_C)}{F_1}\right] + p^3\left[\frac{\tau\, \tau_B\, \tau_C}{F_1}\right]}\right\} \qquad (14)$$

The denominator can be approximately factored as follows:

$$A_{cL} \cong \left\{\frac{R_{f2} + R_{f3}}{p\, C_{f1}\, R_{f3}}\right\} \left\{\frac{p\tau}{\left[1 + p\tau_R(1 + j\alpha)\right]\left[1 + p\tau_R(1 - j\alpha)\right]\left[1 + p^3 \frac{\tau_B\, \tau_C}{F_1\, \tau}\right]}\right\} \qquad (15)$$

where: $$\tau_R \cong \tau\left[1 + \frac{1}{2F_1}\left(1 - \frac{\tau_B\, \tau_C}{\tau^2}\right)\right]$$

$$\alpha = \sqrt{\frac{\tau_B(\tau - \tau_C)}{F_1\, \tau}}$$

Because the third root equal to $\frac{\tau_B\, \tau_C}{F_1\, \tau}$ is typically less than 0.1 μs, its effect on the peak value of the output pulse is less than 1%. Neglecting this root, the output pulse as a function of time for a delta-function charge input is:

$$V_{out} = \left(\frac{Q_D}{C_{f1}}\right)\left(\frac{R_{f2} + R_{f3}}{R_{f3}}\right) \frac{\tau}{\tau_R} \left\{ \frac{\sin\left[\frac{t\alpha}{\tau_R(1+\alpha^2)}\right] \exp\left[\frac{t}{\tau_R(1+\alpha^2)}\right]}{\alpha} \right\} \quad (16)$$

For small values of α, the peak value of the output waveform can be approximated by:

$$V_{peak} \cong \left(\frac{Q_D}{e\, C_{f1}}\right)\left(\frac{R_{f2} + R_{f3}}{R_{f3}}\right) \frac{\tau}{\tau_R} \left(1 - \frac{\alpha^2}{6}\right) \quad (17)$$

Substituting the expressions from equation (15) into equation (17), and keeping only first order terms in $1/F_1$, one obtains for the pulse peak value:

$$V_{peak} \cong \left\{\frac{Q_D}{e\, C_{f1}}\right\}\left\{\frac{R_{f2} + R_{f3}}{R_{f3}}\right\} \left\{1 - \frac{1}{2F_1}\left[1 + \frac{\tau_B}{3\tau}\left(1 - \frac{4\tau_C}{\tau}\right)\right]\right\} \quad (18)$$

The last term represents the correction to the gain caused by finite loop gain and bandwidth. This correction depends on transistor parameters and is highly temperature sensitive.

The gain is also determined by the ratio of R_{f2} to R_{f3} and by the ratio of C_{f2} to C_{f3}. Including first order dependence of the gain on variations of these ratios, the formula for the pulse peak value becomes:

$$Vpeak = \frac{Q_D A_o}{eC_{f1}} \left\{ 1 - \frac{1}{2F_1}\left[1 + \frac{\tau_B}{3\tau}\left(1 - \frac{4\tau_C}{\tau}\right)\right] + \frac{\delta A_o}{2A_o} - \frac{\delta A_1}{2A_1} \right\} \quad (19)$$

where $A_o = \frac{R_{f2}}{R_{f3}}$

$$A_1 = \frac{C_{f2}}{C_{f3}} = \frac{1}{A_o}$$

δA_o = variation of A_o from its nominal value

δA_1 = variation of A_1 from its nominal value

$R_{f2} \gg R_{f3}$

If the effect of finite τ_{f1} is included to first order, the pulse peak value is given by:

$$V_{peak} = \frac{Q_D A_o}{e C_{f1}} \left\{ 1 + E + \frac{\delta A_o}{2A_o} - \frac{\delta A_1}{2A_1} - 0.0766 - 0.144 \left(\frac{\delta \tau_{f1}}{23.3\ \mu s} \right) \right\} \qquad (20)$$

where:

E = transistor parameter dependent gain correction

$$E = - \frac{1.066}{2F_1} \left[1 + \frac{\tau_B}{3\tau} \left(0.963 - \frac{4.22\ \tau_C}{\tau} \right) \right]$$

$\delta\tau_{f1}$ = deviation of τ_{f1} from 23.3 μs

The gain correction dependent on transistor parameters (E) was measured at room temperature as a function of detector capacity and is shown in Figure 11. Measured and theoretical values agree to within about $\pm$ 0.7% for detector capacities up to 350 pF.

Metal film resistors with temperature coefficients less than $\pm$ 25ppM/°C are used for R_{f2} and R_{f3}. The maximum gain drift caused by drifts of these resistors is then less than $\pm$ 0.13% for a $\pm$ 50°C temperature change, with partial temperature tracking of the resistors reducing the drift below this value. Similarly, a metal film resistor is used for R_{f1}, even though such a resistor is physically much larger than a composition carbon resistor. However, a carbon resistor could produce a $\pm$7.5% drift in τ_{f1} resulting in a $\pm$1.1% gain variation over the temperature range. With a metal film resistor for R_{f1} and a glass capacitor for C_{f1}, the drift in τ_{f1} is about $\pm$0.8% over the temperature range, resulting in a gain change of less than $\pm$0.02%.

The gain is inversely proportional to C_{f1}, which is provided by a 4.7 pF glass capacitor in parallel with the 0.4pF capacity associated with R_{f1}. The glass capacitor temperature coefficient, which is specified by the manufacturer* to be fixed within $\pm$5 ppM/°C, has a value of about 120 ppM/°C. A sensistor in series with R_{f2} compensates for the $\pm$0.6% drift in C_{f1} over

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* Corning Glass

the temperature range. The resultant drift produced by lack of perfect tracking of the sensistor and the capacitor and by uncertainties in their temperature coefficients is of the order of $\pm 0.2\%$. Because glass capacitors are also used for C_{f2} and C_{f3}, $\delta A_1/2A_1$ is less than $\pm 0.03\%$ over the temperature range.

Figure 12 shows the measured gain drift with four values of detector capacity for temperatures between -60°C and +100°C. In almost all cases the calculated drifts agreed with the measured drifts within the uncertainties of the temperature coefficients of the gain determining resistors and capacitors. The gain drifts for temperatures between -50°C and +50°C are less than $\pm 0.5\%$ for detector capacities below 350 pF and less than $\pm 1.0\%$ for detector capacities below 540 pF. Holding the amplifier at 145°C for 24 hours with the power off causes gain changes less than $\pm 0.1\%$.

The output resistance for $C_{cl} = 0$ and $C_{cl} = 200$ pF was measured at room temperature by loading the amplifier with a 1K resistor, and observing the difference in output amplitude compared to the unloaded case. The measured output resistances are given in Fig. 13. Loading the amplifier by 1K adds less than $\pm 0.1\%$ to the gain drifts for temperatures between -50°C and +50°C for detector capacities less than 350 pF and less than $\pm 0.2\%$ for detector capacities less than 540 pF.

3.5 Resolution

Because of the large number of carriers produced by most charged particles entering a detector, the energy resolution of an amplifier-detector system is often principally limited by electrical noise. This noise can only be minimized by a thorough understanding of its dependence on the amplifier parameters under the control of the circuit designer.

The largest source of amplifier noise is thermal noise in the channel of the field-effect transistor. Van der Ziel[3] has derived the following approximate formula for the equivalent squared drain noise current per unit bandwidth:

$$\overline{i_d^2} = 4kTg_m \tag{21}$$

where: k = Boltzman's constant = 1.38×10^{-23} j/°K

T = temperature in degrees Kelvin

g_m = transconductance in mho

and the bandwidth is measured in cycles per second

This noise current source may be replaced by an equivalent voltage source $\overline{e_d^2}$ inserted between the source and ground.

Then:

$$\overline{e_d^2} = \frac{\overline{i_d^2}}{g_m^2} = \frac{4kT}{g_m} \tag{22}$$

Using the complex gain given by equation (2), the squared output noise per unit bandwidth $d(\overline{V_d^2})$ resulting from the channel thermal noise is:

$$d(\overline{V_d^2}) = \overline{e_d^2}\left(\frac{C_D + C_B}{C_{f1}}\right)^2\left(\frac{R_{f2}}{R_{f3}}\right)^2\left|\frac{j\omega\tau}{(1 + j\omega\tau)^2}\right|^2 \frac{d\omega}{2\pi} \tag{23}$$

Integrating this expression over all frequencies, the total squared output noise is given by:

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(3) A Van der Ziel, "Thermal Noise in Field-Effect Transistors", Proc. IRE, Vol. 50, pp. 1808-1812, August 1962

$$\overline{V_d^2} = \overline{e_d^2}\left(\frac{C_D + C_B}{C_{f1}}\right)^2\left(\frac{R_{f2}}{R_{f3}}\right)^2 \frac{1}{2\pi\tau}\int_0^\infty \frac{X^2\,dX}{(1+X^2)^2} \qquad (24)$$

where: $X = \omega\tau$

and the value of the integral is $\frac{\pi}{4}$.

If the squared output noise voltage is divided by the square of the conversion gain, given in equation (3), then the squared equivalent input energy $\overline{E_{nd}^2}$ is:

$$\overline{E_{nd}^2} = \frac{\overline{e_d^2}\,(C_D + C_B)^2}{8\tau}\left(\frac{e\,E_o}{q}\right)^2 \qquad (25)$$

The actual drain noise current is larger than the value quoted by Van der Ziel by a factor ranging from 1.3 to 4, depending on the specific transistor being used. In terms of the actual equivalent squared noise voltage per unit bandwidth $\overline{e_n^2}$, the input noise may be written:

$$\overline{E_{nd}^2} = \frac{\overline{e_n^2}\,(C_D + C_B)^2}{\tau}\ (4.46 \times 10^{32}) \qquad (26)$$

where capacitor values are in farads and times are in seconds.

Statistical fluctuations in the gate leakage current generate an equivalent squared noise current per unit bandwidth $\overline{i_g^2}$ given by:

$$\overline{i_g^2} = 2qI_g \qquad (27)$$

where: I_g = gate leakage current in amperes

The equivalent squared input noise $\overline{E_g^2}$ resulting from this effect is:

$$\overline{E_g^2} = \frac{\overline{i_g^2}\,\tau}{2\pi}\left(\frac{eE_o}{q}\right)^2 \int_o^\infty \frac{dX}{(1+X^2)^2} \qquad (28)$$

where the value of the integral is $\frac{\pi}{4}$. The input RMS noise current per

unit bandwidth is specified by the manufacturer * for the 2N2500, and agrees with equation (27) with $I_g = 5 \times 10^{-10}$A at frequencies near 100 c/s. However, as frequency increases, this noise current increases slowly so that at frequencies near 100 Kc/s an extrapolation of the manufacturer's data and an attempt to fit the measured amplifier noise for zero detector capacity gives:

$$\sqrt{\overline{i_n^2}} = 6\sqrt{\overline{i_g^2}} = 9 \times 10^{-14} \text{ A } (c/s)^{-\frac{1}{2}} \qquad (29)$$

Where: $\overline{i_n^2}$ = squared noise per unit bandwidth as measured by the manufacturer and extrapolated to 100 Kc/s.

Temperature = 25°C

Substituting these values into equation (28), the resulting equivalent squared input noise energy is:

$$\overline{E_{ng}^2} = \overline{i_n^2}\,\tau\,(4.46 \times 10^{32}) = (3.62 \times 10^6)\,\tau \quad (KeV)^2 \qquad (30)$$

The detector and field-effect bias resistors are also thermal noise sources. Because the bandwidth calculation for these noise sources is the same as for the gate leakage current, the equivalent squared input noise energy from these resistors is:

$$\overline{E_{nr}^2} = \overline{i_r^2}\,\tau\,(4.46 \times 10^{32}) \quad (KeV)^2 \qquad (31)$$

where:

$$\overline{i_r^2} = \frac{4kT}{R_D} \qquad (32)$$

For $R_D = 4.06M$ and

$T = 25°C = 298°$ K:

Then:

$$\overline{E_{nr}^2} = (1.76 \times 10^6)\,\tau \quad (KeV)^2 \qquad (33)$$

* Texas Instruments

The resistor (R_{c3}) in series with the detector also produces thermal noise given by:

$$\overline{E_{nc}^2} = \frac{4kT\,\tau_{c3}\,C_D}{2\pi\tau}\left(\frac{e\,E_o}{q}\right)^2 \int_0^{\infty} \frac{X^2\,dX}{\left[1+\left(\frac{\tau_{c3}}{\tau}\right)^2 X^2\right]\left[1+X^2\right]^2} \qquad (34)$$

Because τ_{c3} is small compared to τ, the approximate value of the integral is $\pi/4$, yielding:

$$\overline{E_{nc}^2} = \frac{7.14 \times 10^4\, C_D}{\tau} \qquad (KeV)^2 \qquad (35)$$

for $\tau_{c3} = 10$ ns

$T = 25°C = 298°$ K

The total RMS equivalent noise energy for the amplifier is then:

$$\sqrt{\overline{E_{na}^2}} = \sqrt{\overline{E_{nd}^2} + \overline{E_{ng}^2} + \overline{E_{nr}^2} + \overline{E_{nc}^2}} \qquad (36)$$

For $\tau = 2\mu$s, the total noise becomes:

$$\sqrt{\overline{E_{na}^2}} = \sqrt{(2.23 \times 10^{38})(C_D + 15\text{pF})^2\ \overline{e_n^2} + (3.57 \times 10^{10})\ C_D + 10.76} \quad (KeV)$$

The quantity $\overline{e_n^2}$ was determined for several field effect transistors by measuring the output noise using a true RMS voltmeter* with a 158 pF capacitor placed across the amplifier input. Because the amplifier has a conversion gain of 1V/MeV, the RMS output noise voltage becomes:

$$\sqrt{\overline{V_{na}^2}} = \sqrt{6.67 \times 10^{18}\ \overline{e_n^2} + 16.4} \qquad (mV) \qquad (37)$$

* Ballentine Model 320

Figure 14 shows the noise distribution of 25 transistors at room temperature. As would be expected, units exhibiting a large g_m also appear to be the most quiet. However, even among the high g_m units, the equivalent noise voltage varies 2 to 1. The only conclusion is that other sources besides channel thermal noise may contribute to the total noise. From 25 transistors six satisfy the current and transconductance requirements for laboratory use and are low noise units ($\sqrt{\overline{e_n^2}} \leq 5.0 \times 10^{-9}$ V $(c/s)^{-\frac{1}{2}}$), while two low noise units are suitable for spacecraft applications. ** These results are summarized in Table 2. Care should be exercised in extrapolating yields from a sample this small.

A unit with an equivalent noise voltage of 4.15×10^{-9} V $(c/s)^{-\frac{1}{2}}$ was used in an amplifier constructed to test the noise theory. Figure 15 shows the calculated and measured noise versus detector capacity with $\tau_{c3} = 10$ ns. The equivalent noise voltage ($\overline{e_n^2}$) and the equivalent noise current ($\overline{i_n^2}$) were determined as discussed above. No change in the noise was observed after the transistor had been at 145°C for 24 hours with the power off or after repeated testing with power on at temperatures from -60°C to +100°C.

The detector itself also is a principal contributor to the resolution[4]. In addition to capacitive effects, the detector produces noise resulting from statistical variations of the leakage current ($\overline{E_{nl}^2}$) and in the number of carriers released ($\overline{E_{nq}^2}$). The resolution is further spread by variations in collection efficiency and in detector uniformity ($\overline{E_{nu}^2}$). The total detector resolution $\overline{E_{nd}^2}$ can be then written as:

$$\overline{E_{nd}^2} = \overline{E_{nl}^2} + \overline{E_{nq}^2} + \overline{E_{nu}^2} \qquad (38)$$

The leakage current noise is related to the amplifier pulse shaping in the same way as the field-effect transistor leakage, namely:

** 2N2497 transistors selected by Texas Instruments for $g_m \geq 1500$ μmho at $I_D = 1$mA and $I_{DSS} \geq 2.0$ mA are available as special product SM5688.

(4) Semiconductor Particle Detectors - J. M. Taylor, Butterworths, Inc. 1963

$$\overline{E_{nl}^2} = (I_L \tau)(1.43 \times 10^{14}) \quad (KeV)^2 \quad (38a)$$

where I_L = detector leakage current in amperes

The variation in the number of carriers released is given by Poisson statistics and thus:

$$\overline{E_{nq}^2} = E E_o \quad (KeV)^2 \quad (38b)$$

where: E = energy loss in depletion layer in KeV

E_o = energy per ion pair = 3.5×10^{-3} KeV

Combining both detector and amplifier resolutions, the total RMS energy resolution may be expressed as:

$$\sqrt{\overline{E_{nt}^2}} = \sqrt{\overline{E_{na}^2} + \overline{E_{nd}^2}} \tag{39}$$

or in terms of the full width at half maximum counting rate:

$$FWHM = 2.35\sqrt{\overline{E_{na}^2} + \overline{E_{nd}^2}} \tag{40}$$

Figure 15 also shows the calculated total energy resolution assuming a 25 KeV (FWHM) resolution for the detector. This resolution was checked directly using an Am^{241} source, whose spectrum near the principal peak is listed in Table 3. The resulting peaks for two detectors are shown in Figure 16. Because of the low energy tail caused by α emission to excited states and by scattering from the walls, the resolution was calculated by doubling the upper half width at half maximum. The amplifier gain, which was measured to be 0.98 V/MeV, is within the tolerances of the gain determining elements. The calculated and measured resolutions are compared in Figure 15.

For applications where resolution is most critical, further optimization is possible by varying the shaping time constant and by providing additional pulse shaping. The total resolution may be expressed as:

$$\overline{E_{nt}^2} = \overline{E_{nq}^2} + \overline{E_{nu}^2} + \frac{K_D D}{\tau} + K_E E \tau \tag{41}$$

where: $D = (7.73 \times 10^{-3})(C_D + 15)^2 + 7.14 \times 10^{-2}\, C_D$ $\quad (KeV)^2(\mu s)$

$E = 143\, I_L + 5.38$ $\quad (KeV)^2(\mu s)^{-1}$

K_D, K_E = constants determined by the number of clipping and integrating time constants

C_D = detector capacity in picofarads.

I_L = detector leakage current in microamperes.

τ = clipping and integrating time constants in microseconds

The best resolution results when the shaping time constant is:

$$\tau_{opt} = \sqrt{\frac{K_D D}{K_E E}} \tag{42}$$

Then the resultion has a value given by:

$$\overline{E_{opt}^2} = \overline{E_{nq}^2} + \overline{E_{nu}^2} + 2\sqrt{K_D K_E\, DE} \tag{43}$$

For one clipping time constant and one integrating time constant:

$$K_D = K_E = 1$$

$$\tau_{opt} = \sqrt{\frac{D}{E}}$$

$$\overline{E_{opt}^2} = \overline{E_{nq}^2} + \overline{E_{nc}^2} + 2\sqrt{DE} \tag{44}$$

In Figure 17, τ_{opt} and $\sqrt{\overline{E_{opt}^2}}$ are plotted versus detector capacity for a leakage current of 0.1 μA. The resolution for a constant 2 μs shaping time constant is shown for comparison.

For one clipping time constant combined with two equal integrating time constants then:

$$K_D = 0.465$$

$$K_E = 1.40 \tag{45}$$

and the conversion gain is reduced to 0.73 V/MeV. For this case:

$$\tau_{opt} = 0.576\sqrt{\frac{D}{E}}$$

$$\overline{E_{opt}^2} = \overline{E_{nq}^2} + \overline{E_{nc}^2} + (0.806)\,(2\sqrt{DE}) \tag{46}$$

For one integrating time constant combined with two equal clipping time constants,

$$K_D = 1.9$$
$$K_E = 0.637 \qquad (47)$$

and the conversion gain becomes 0.63 V/MeV. In this case:

$$\tau_{opt} = 1.73\sqrt{\frac{D}{E}} \qquad (48)$$

$$\overline{E^2_{opt}} = \overline{E^2_{nq}} + \overline{E^2_{nc}} + (1.1)\,(2\sqrt{DE})$$

Naturally if the shaping time constant is varied, the high frequency compensation will have to be changed accordingly. If the shaping time constant becomes too short, excessive gain drifts may result. Conversely, long shaping time constants may cause difficulty with tail pile-up at high repetition rates.

Figure 18 illustrates the dependence of amplifier noise on temperature. For temperatures below about 70°C, field-effect transistor channel noise dominates, and the noise is roughly proportional to the absolute temperature. Above 70°C, gate leakage current, which rises exponentially with temperature, becomes significant. For detectors having leakage currents of about 0.1μA at room temperature, the exponential rise of noise with temperature would probably begin near 50°C.

IV. DISCRIMINATOR

4.1 General

Figure 19 shows a complete schematic of a discriminator with a threshold equal to a DC bias voltage. For bias voltages between 0.1V and 5V, better than 1% threshold stability is obtained using pulses produced by the amplifier with shaping time constant greater than or equal to 0.5μs. This discriminator is considered the most versatile version, and some simplification of the circuit may be possible for less demanding requirements.

A block diagram is shown in Figure 20. Basically, the circuit consists of a single shot preceded by a window amplifier with a variable bias. The single shot uses a complimentary flip-flop output stage in which both logical states are clamped by a saturated transistor to either ground or the -6V supply, providing low output impedance, fast (0.2μs) rise and fall times without large standing currents, small sensitivity to noise and pickup, and stable output voltages. A photograph of the discriminator output pulse is shown in Figure 21. Because the threshold of the complimentary flip-flop is highly sensitive to transistor gains and diode voltages, the flip-flop is preceded by a differential amplifier. Both are biased so that the flip-flop triggers approximately when the differential stage is balanced and thus most stable. Positive feedback via series RC circuits to both sides of the difference amplifier determines the output pulse width.

A window amplifier is placed before the single shot in order to improve the threshold stability for small signals and to provide a convenient place for a variable bias which does not effect the output pulse width. Because the single shot is biased to trigger when the window amplifier is also balanced, and because the transistors are matched so that equal currents occur for base voltages equal to within ± 3mV, the threshold for small signals of long duration equals the initial voltage on the base of Q1a to within about ±3mV. Because Q1a is normally cut off by the bias voltage, the input impedance is given by the 10K bias resistor, the size of which is only limited by the voltage shifts caused by transistor leakage currents. For biases less than 80mV, Q1a starts to conduct, resulting in base current flowing in the bias resistor, amd a smaller value of this resistor must be

used for stable operation. Most of the drifts for bias voltages in excess of 1V arise from the non-zero response time of the single shot. In order to reduce this response time as much as possible without large standing currents and consequential waste of power, fast switching transistors are used for the complimentary flip-flop, and diodes limit the voltage swings at the collectors of Q1 and Q2 and at the bases of Q4 and Q6.

4.2 Triggering Sequence

The discriminator has two states, one of which is stable and the other is not. The transition from the stable state to the unstable state constitutes "triggering", and the size of the pulse which just barely causes triggering determines the threshold. Because the stability of the threshold depends on the sequence of events leading to triggering, this sequence must first be understood in detail.

In the stable state, transistor Q_{1a} (see Figure 19) is cut-off by the bias voltage, resulting in Q_{2b} and CR_1 conducting with Q_{2a} and CR_2 cut-off. Because Q_{2b} is conducting, Q_5 is saturated, resulting in Q_4 also being saturated. The OUT signal is thus clamped to ground, while the $\overline{OUT}$ signal is clamped to -6V.

When a sufficiently large pulse is applied to the input, the base voltage of Q_{1a} is raised to near zero volts, causing Q_{1a} to conduct and reducing the current in Q_{1b}. When the currents in Q_{1a} and Q_{1b} become nearly equal, Q_{2a} starts to conduct, decreasing the current in Q_{2b} by the same amount. As a result, Q_5 and CR_3 stop conducting, and the voltage on the base of Q_3 begins to rise and base drive is no longer supplied to Q_5. Nevertheless, its collector voltage does not rise immediately because of the stored charge in Q_4 and Q_5. This stored charge can only be quickly removed by a large collector current either supplied by loading or by the conduction of Q_3 and Q_6. As a result, the circuit triggers for short pulses before Q_3 conducts only if the OUT signal is loaded to -6V or the $\overline{OUT}$ signal is loaded to ground by several milliamperes.

Although positive feedback via C_{f2} and R_{f2} tends to increase the current in Q_{2a}, this feedback is inoperative for short times. Because the stored charge in Q_4 and Q_5 effectively clamps the $\overline{OUT}$ signal at -6V, no signal is fedback until this charge is removed. In addition, the slow response

time of the differential amplifier (Q_2) caused by collector-base capacity prevents rapid regeneration (see section 4.3).

The voltage on the base of Q_3 continues to rise until Q_3 starts to conduct. The collector current of Q_3 then rapidly clears the stored charge from Q_4, and the OUT signal begins to fall. This signal is coupled to the base of Q_6 via a 100pF capacitor, and, after falling by about 1.4V, begins to bring Q_6 into conduction. The collector current of Q_6 then rapidly pulls the $\overline{OUT}$ signal positive. When the OUT and $\overline{OUT}$ signals have moved about 3V, the feedback currents via R_{f1} and R_{f2} are sufficient to hold Q_{2a} conducting and Q_{2b} off independently of the input signal. At this time triggering has occurred because the circuit proceeds inevitably to the unstable state.

The minimum load resistance is determined primarily by the base drive of Q_4 and Q_6 and their current gain at -50°C. If Q_4 and Q_6 are selected to have current gains of 100 at room temperature, their gain at -50°C will be about 50. For the base drive of 0.18mA, a collector current of 9mA will be available. In order to allow some margin of safety, the load current should not exceed about 6mA, implying a minimum load resistance of 1K to voltages between ground and -6V.

If the input pulse does not hold Q_{1a} conducting, the time of the transition from the unstable state back to the stable state is determined by the charging of the feedback timing capacitors (C_{f1} and C_{f2}). Typically, this output pulse width is made sufficiently long so that the amplifier pulse has become negative before the discriminator attempts to return to the stable state and thus Q_{1a} is guaranteed to be cut-off. This time for a 2μs shaping time constant is 8μs (see Fig. 2).

The return to the stable state occurs approximately in the reverse sequence as triggering. The collector currents in Q_{2a} and Q_{2b} are nearly equal at this time, and, because the transistors are matched to have qual base voltages for equal collector currents, the return transistion occurs when the base voltages are qual. Thus, the pulse width T is given by:

$$T = \tau_f \left\{ \ln \left(\frac{2V_o}{R_f I_1} \right) + V_D \left(\frac{1}{R_f I_1} - \frac{1}{V_o} \right) \right\} \qquad (49)$$

where: $\tau_f = R_{f1}C_{f1} = R_{f2}C_{f2}$

V_o = output voltage = 5.5V

I_1 = collector current in Q_{1b} = 0.4mA

$R_f = R_{f1} = R_{f2}$ = 13K

V_D = forward voltage drop of CR_1 and CR_2

For the values shown in Figure 19:

$$T = 9.76\ C_f \left[1 + 0.0133\ V_D \right] \qquad \text{(ns)} \qquad (50)$$

for C_f in picofarads and V_D in volts. For V_D equal to 0.7V, then:

$$T = 9.85 C_f \qquad \text{(ns)} \qquad (51a)$$

A comparison of this formula with measured results is shown is Figure 22.

The diode forward voltage drifts by 0.25V for temperatures between -50°C and +50°C, while I_1 varies by about 1.5%, producing a drift in the pulse width of 2.5%. The timing capacitors and resistors also vary about 1%, resulting in a total drift of the pulse width of less than 3.5%. Measurements show an increase in pulse width at -50°C to 4.4μs for a width of 4.3μs at +50°C.

4.3 Threshold Stability

Preliminary measured drifts of the threshold for temperatures between -50°C and +50°C are shown in Figure 23. These results agree roughly with calculated estimates of the drifts. These calculations and final drift measurement will be present in the completed report.

TABLE I - TYPICAL VALUES

		C_D = 100 pF, C_{C1} = 17.5 pF			C_D = 1 pF, C_{C1} = 500 pF		
TEMPERATURE (°C)		-50	+25	+50	-50	+25	+50
F_o	X10^5	4.75	7.08	5.72	4.75	7.08	5.72
τ_A	μs	310	334	322	100	124	112
τ_B	μs	16.9	23.3	25.7	15.9	19.2	23.4
τ_C	ns	299	296	314	689	892	959
τ_D	ns	10.5	10.5	10.5	10.5	10.5	10.5
τ_E	ns	54	60	61	54	60	61
τ_F	ns	3.5	4.0	4.2	3.5	4.0	4.2
τ_G	ns	17	11.3	11.3	17	11.3	11.3
τ_H	ns	8.5	8.0	8.0	2.9	1.0	1.0
τ_I	ns	1.3	1.3	1.3	0	0	0
τ_J	ns	1.8	2.4	2.6	1.8	2.4	2.6
τ_K	μs	540	540	540	540	540	540
τ	μs	2.0	2.0	2.0	2.0	2.0	2.0
τ_{f1}	μs	23	23	23	23	23	23
τ_{c1}	ns	10	10	10	10	10	10
τ_{c2}	ns	30	30	30	30	30	30
τ_{c3}	ns	10	10	10	0	0	0
R_{c2}	Ω	570	570	570	20	20	20
R_{c3}	Ω	100	100	100	0	0	0
R_D	M Ω	4.0	4.0	4.0	4.0	4.0	4.0
C_A	pF	46.4	57.4	52	46.4	57.4	52
C_B	pF	15	15	15	15	15	15
g_m	μmho	2210	1700	1530	2210	1700	1530
r_{e2}	Ω	35	45	49	35	45	49
r_{e3}	Ω	48	63	68	48	63	68
r_{e4}	Ω	27	35	37	25	35	37
r_d	K Ω	80	80	80	80	80	80
β_2		185	450	530	185	450	530
β_3		185	450	530	185	450	530
β_4		50	100	110	50	100	110
C_{ob}	pF	3.3	3.3	3.3	3.3	3.3	3.3
τ_{T2}	ns	2.0	2.0	2.0	2.0	2.0	2.0
τ_{T3}	ns	2.0	2.0	2.0	2.0	2.0	2.0
τ_{T4}	ns	0.2	0.2	0.2	0.2	0.2	0.2
R_L	K Ω	3.3	3.3	3.3	3.3	3.3	3.3
C_L	pF	200	200	200	200	200	200

TABLE II

FIELD-EFFECT TRANSISTOR SELECTION

SELECTION CRITERIA	2N2497	2N2500
Total number of transistors investigated	18	7
$I_{DSS} \geq 1.5$ mA	14	7
$I_{DSS} \geq 2.0$ mA	7	7
$I_{DSS} \geq 1.5$ mA $g_m \geq 1500$ μmho	6	3
$I_{DSS} \geq 2.0$ mA $g_m \geq 1500$ μmho	2	3
$I_{DSS} \geq 1.5$ mA $g_m \geq 1500$ μmho $\sqrt{\overline{e_n^2}} \leq 5 \times 10^{-9} V(C/S)^{-\frac{1}{2}}$	5	1
$I_{DSS} \geq 2.0$ mA $g_m \geq 1500$ μmho $\sqrt{\overline{e_n^2}} \leq 5 \times 10^{-9} V(C/S)^{-\frac{1}{2}}$	1	1

I_{DSS} = Drain Current for:
$V_{gs} = 0$; $V_{ds} = -5V$
g_m = Transconductance for:
$I_D = 1$ mA; $V_{ds} = -5V$

TABLE III

Alpha Particle Energy Spectrum of Am^{241} Near the Major Peak (5)

Energy (MeV)	% of Total
5.534	0.35
5.500	0.23
5.477	85
5.435	12.6
5.378	1.7
5.311	0.012

(5) D. Strominger, J. M. Hollander, and G. T. Seaborg, Rev. Mod. Phys., Vol. 30, No. 2, Part 2, Apr. 1958, p 826.

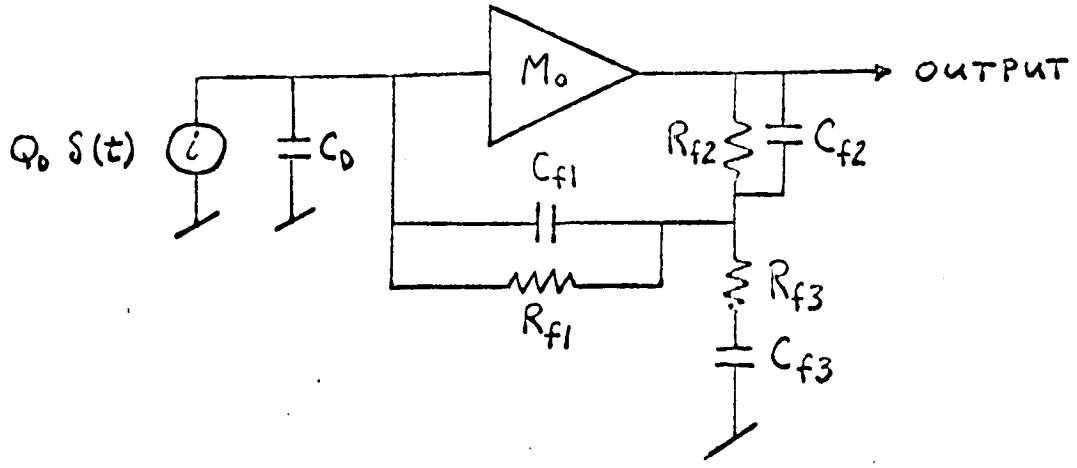


FIGURE 1
AMPLIFIER SIMPLIFIED SCHEMATIC

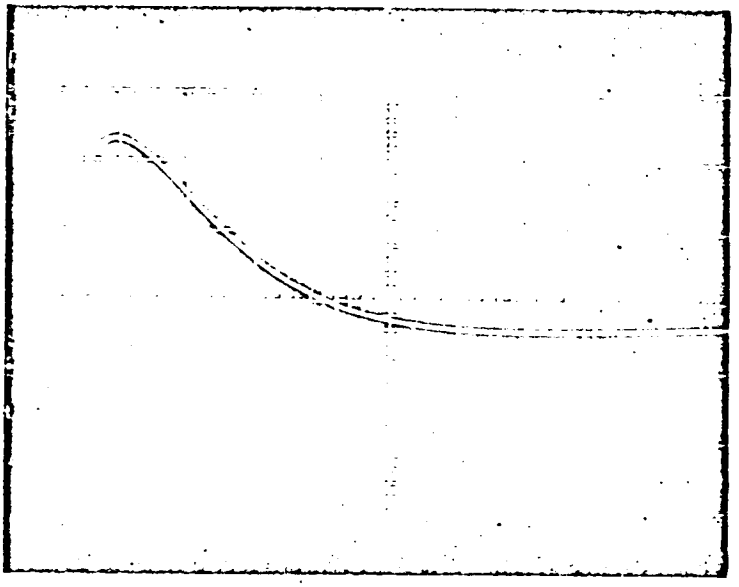


Fig. 2 - Amplifier Output Pulse

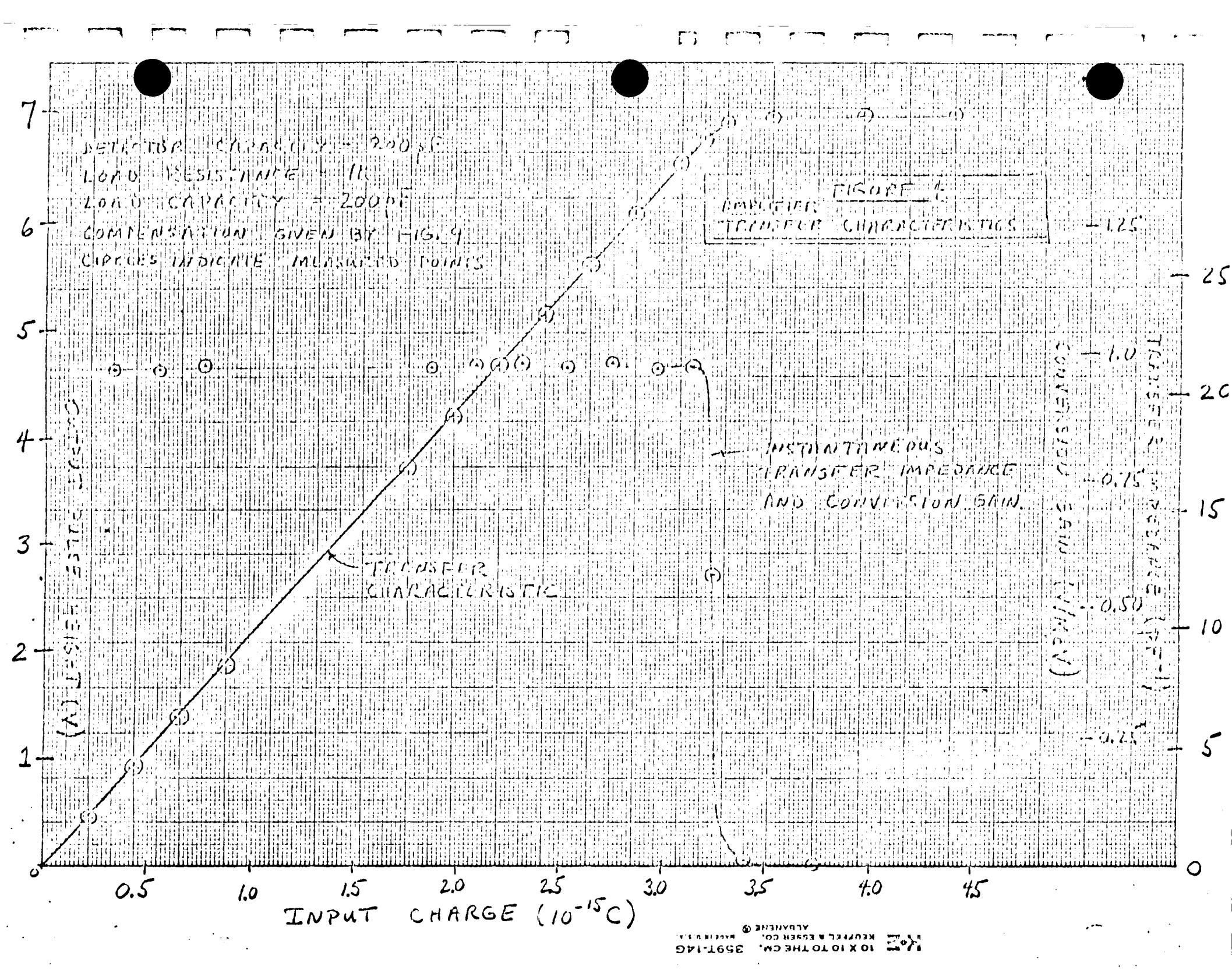
Horizontal: 2μs/cm
Verticle: 2 V/cm

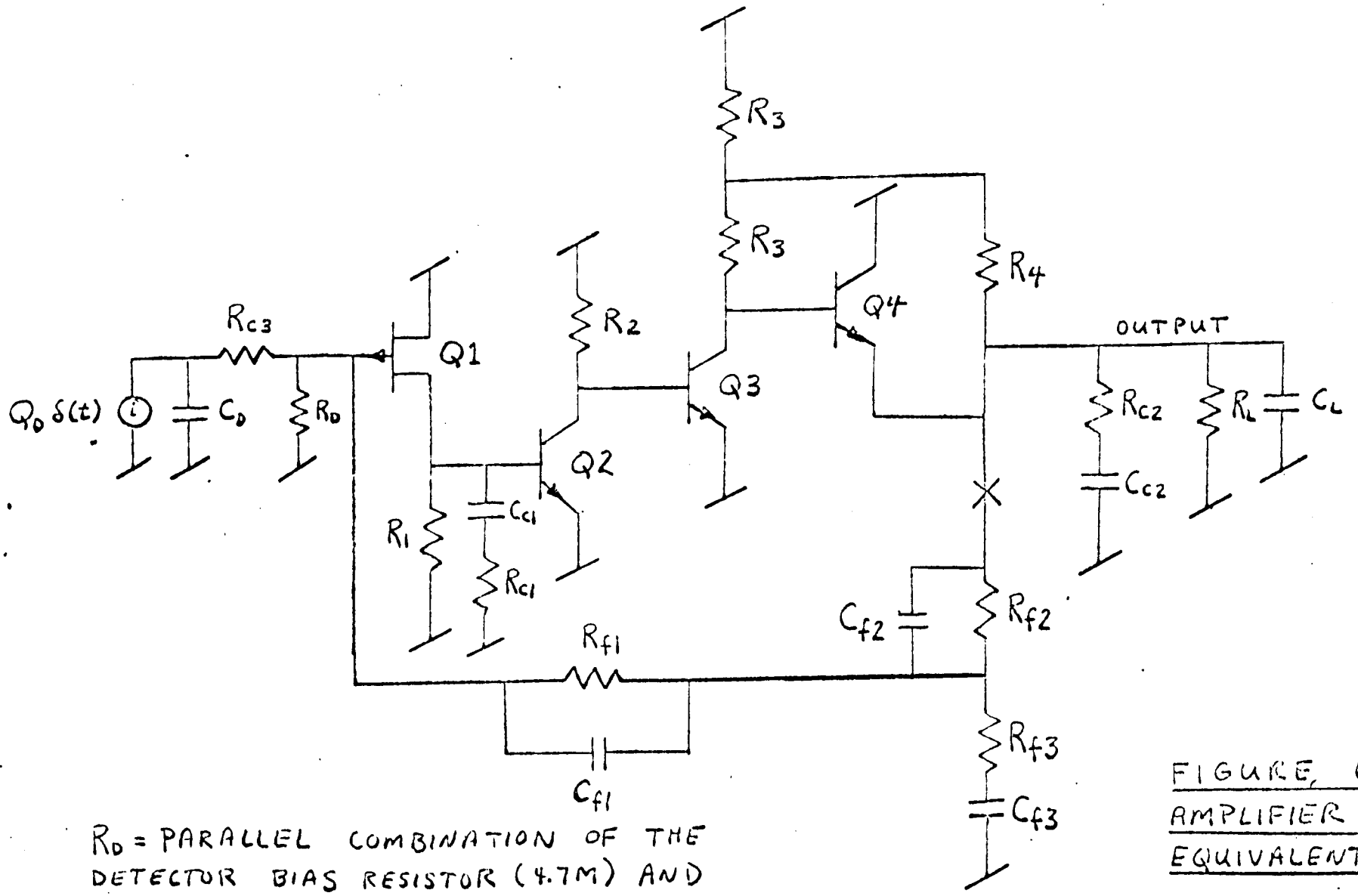
NOTES FOR LABORATORY VERSION

1. $R_{c1} = 56.2\ \Omega$, $R_{c3} = 100\ \Omega$, and $C_{c1} = 200$ pF.
   Compensation must be in for detector capacity less than 50 pF.
2. Select for $I_c \geq 1.5$ mA at $I_B = 0.02$ mA, $V_{CE} = 5V$ ($\beta \geq 75$). TO-18 Can.
3. All resistors IRC RN60C, unless otherwise noted. All capacitors less than 1000 pF El-Menco Silver Mica, temperature characteristic E, unless otherwise noted.
4. Select for $I_C \geq 0.6$ mA at $I_B = 0.002$ mA, $V_{CE} = 5V$ ($\beta \geq 300$). Q_2 and Q_3 are in the same TO-18 can, which should be grounded near the emitter of Q_3.
5. Select for $I_{DC} \geq 1.5$ mA at $V_{GS} = 0$, $V_{DS} = -5V$. $G_m \geq 1500$ at $I_{DS} = 1.0$ mA, $V_{DS} = -5V$. Low noise unit (see Sect. 3.5). TO-5 Can.
6. Circled numbers refer to common ground points.
7. $R_{c4} = 1.0K$
8. Keep indicated leads as short as possible.
9. Match R_B to Q_1 so that the emitter of Q_4 is at 3.4V.
10. Use values shown for general purpose operation.
11. 0.15μF - 100 VDC, Sprague CP 08A1KB154K capacitor may be used to filter 60 c/s ripple on detector power supply.
12. Omit these components if the calibration input is not required.
13. Match C_{f1} to the capacity across R_{f1} so that the total capacity is 5.1 pF $\pm$ 1%.

NOTES FOR SPACECRAFT VERSION

1. See Fig. 9 for values of R_{c1}, R_{c3}, and C_{c1} as a function of detector capacity. Omit switch.
2. Select for $I_C \geq 2.0$ mA at $I_B = 0.02$ mA, $V_{CE} = 5V$ ($\beta \geq 100$). TO-18 Can.
3. All Resistors IRC RN60C, unless otherwise noted. All capacitors less than 1000 pF El-Menco Silver Mica, temperature characteristic E, unless otherwise noted.
4. Select for $I_C \geq 0.8$ mA at $I_B = 0.002$ mA, $V_{CE} = 5V$ ($\beta \geq 400$). Q_2 and Q_3 are in the same TO-18 Can, which should be grounded near the Emitter of Q_3.
5. Select for $I_{DS} \geq 2.0$ mA at $V_{GS} = 0$, $V_{GD} = -5V$. $G_M \geq 1500$ at $I_{DS} = 1.0$ mA, $V_{DS} = -5V$. Low Noise unit (See Sect. 3.5). TO-5 Can.
6. Circled numbers refer to common ground points.
7. Adjust to desired dynamic range according to EQ.6. $R_{C4} \geq 1.0K$.
8. Keep indicated leads as short as possible.
9. Match R_B to Q_1 so that the emitter of Q_4 is at 3.4V.
10. Omit 10μF, 46.7Ω, and 100K. Connect output directly to circuits with capacitively coupled inputs. Capacitively couple with 200μs time constant to circuits with DC coupled inputs.
11. 0.01μF should be sufficient for most applications.
12. Omit these components if the calibration input is not required.
13. Match C_{f1} to the capacity across R_{f1} so that the total capacity is 5.1 pF ± 1%.

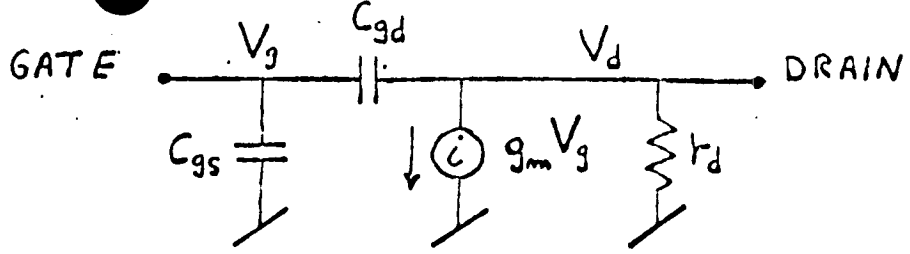

DETECTOR CAPACITY = 200pF
LOAD RESISTANCE = ∞
LOAD CAPACITY = 200pF
COMPENSATION GIVEN BY FIG. 4
CIRCLES INDICATE MEASURED POINTS
FIGURE 4
AMPLIFIER TRANSFER CHARACTERISTICS
INSTANTANEOUS TRANSFER IMPEDANCE AND CONVERSION GAIN.
TRANSFER CHARACTERISTIC
OUTPUT VOLTAGE (VOLTS)
INPUT CHARGE (10^{-15}C)
CONVERSION GAIN (VOLTS/e⁻)
TRANSFER IMPEDANCE (MEGOHMS)
0
1
2
3
4
5
6
7
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
0.25
0.50
0.75
1.0
1.25
5
10
15
20
25



R_D = PARALLEL COMBINATION OF THE DETECTOR BIAS RESISTOR (4.7M) AND THE FIELD-EFFECT TRANSISTOR BIAS RESISTOR (30.1M)

FIGURE 6
AMPLIFIER AC EQUIVALENT CIRCUIT

GROUNDED SOURCE FIELD-EFFECT TRANSISTOR



g_m = TRANSCONDUCTANCE = $g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}$

r_d = DRAIN OUTPUT RESISTANCE

I_D = DC DRAIN CURRENT

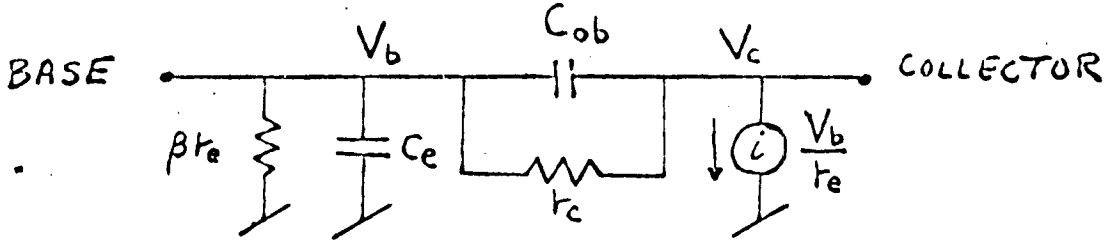
I_{DSS} = DRAIN CURRENT FOR $V_g = 0$

g_{mo} = TRANSCONDUCTANCE FOR $V_g = 0$

C_{gs} = GATE-SOURCE CAPACITY

C_{gd} = GATE-DRAIN CAPACITY

GROUNDED EMITTER BIPOLAR TRANSISTOR



r_e = GROUNDED-BASE EMITTER INPUT RESISTANCE (h_{ib}) = $\frac{kT}{qI_e} + r_b$

k = BOLTZMAN'S CONSTANT

T = ABSOLUTE TEMPERATURE

q = CHARGE ON THE ELECTRON

I_e = DC EMITTER CURRENT

r_b = BASE SPREADING RESISTANCE REFERRED TO THE EMITTER

β = GROUNDED-EMITTER FORWARD CURRENT GAIN (h_{fe})

r_c = GROUNDED-BASE COLLECTOR OUTPUT RESISTANCE (h_{ob})

C_{ob} = GROUNDED-BASE COLLECTOR OUTPUT CAPACITY

$C_e = \frac{\tau_T}{r_e} \approx \frac{1}{2\pi f_T r_e}$

f_T = CURRENT GAIN-BANDWIDTH PRODUCT

FIGURE 7
TRANSISTOR AC
EQUIVALENT CIRCU

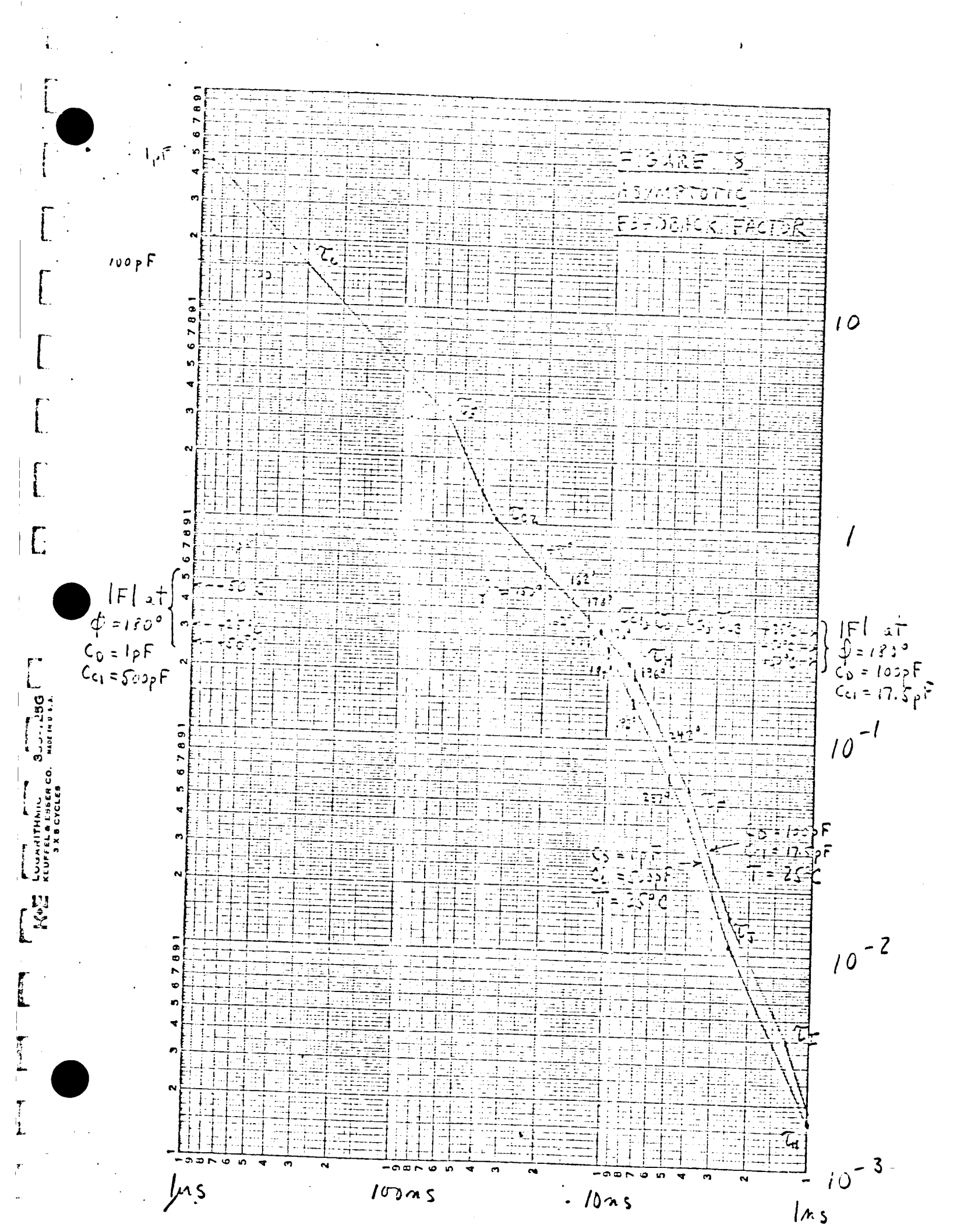
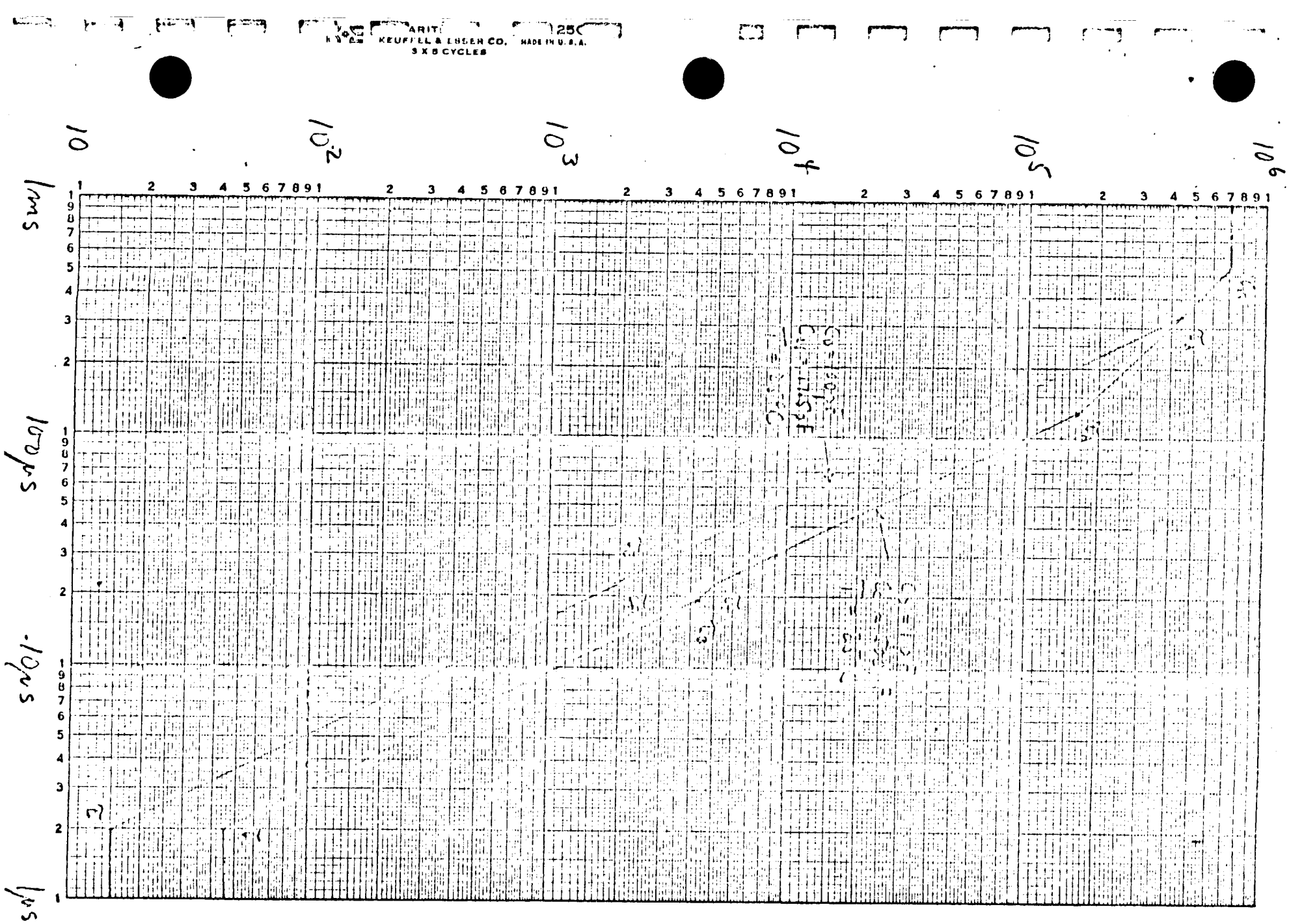
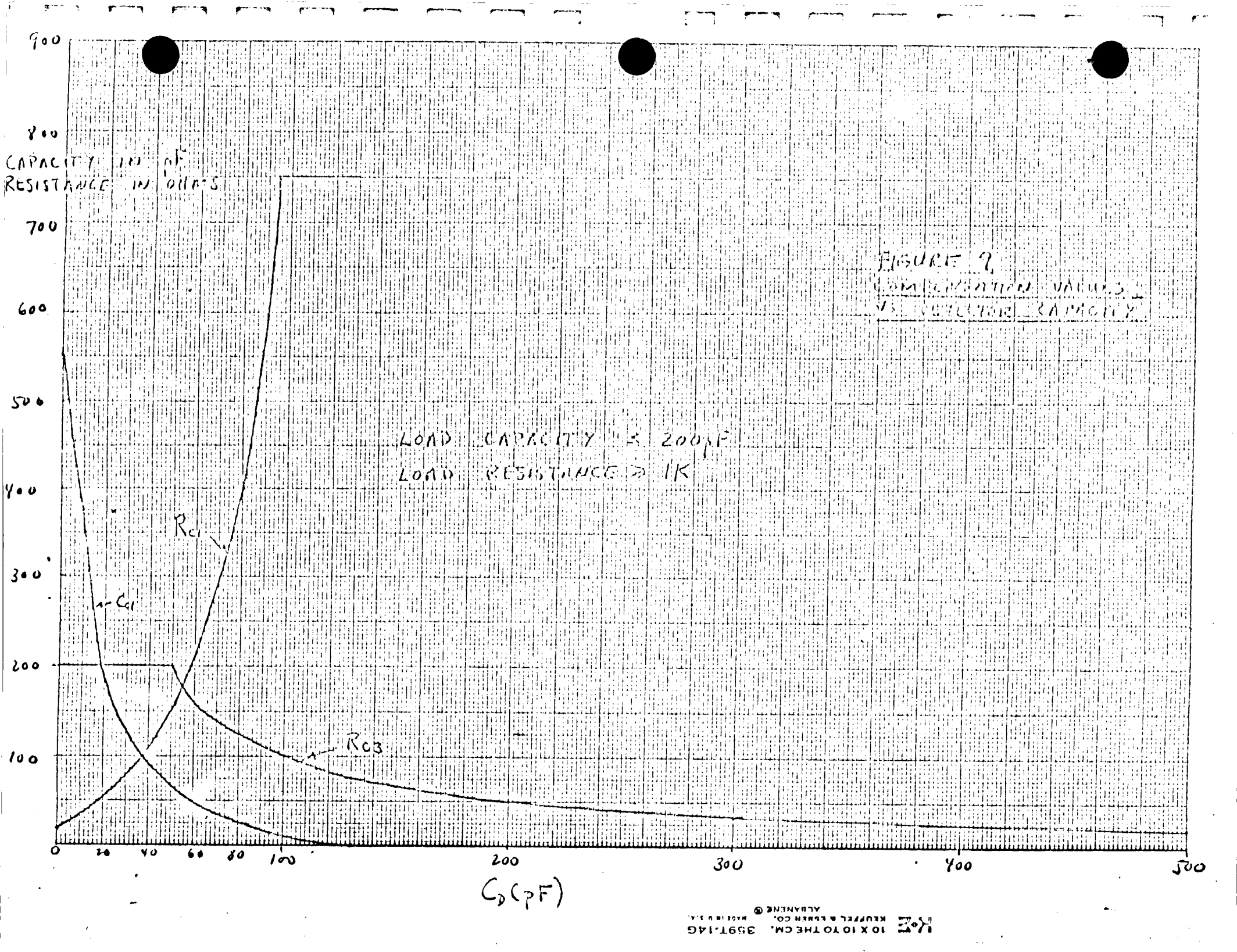
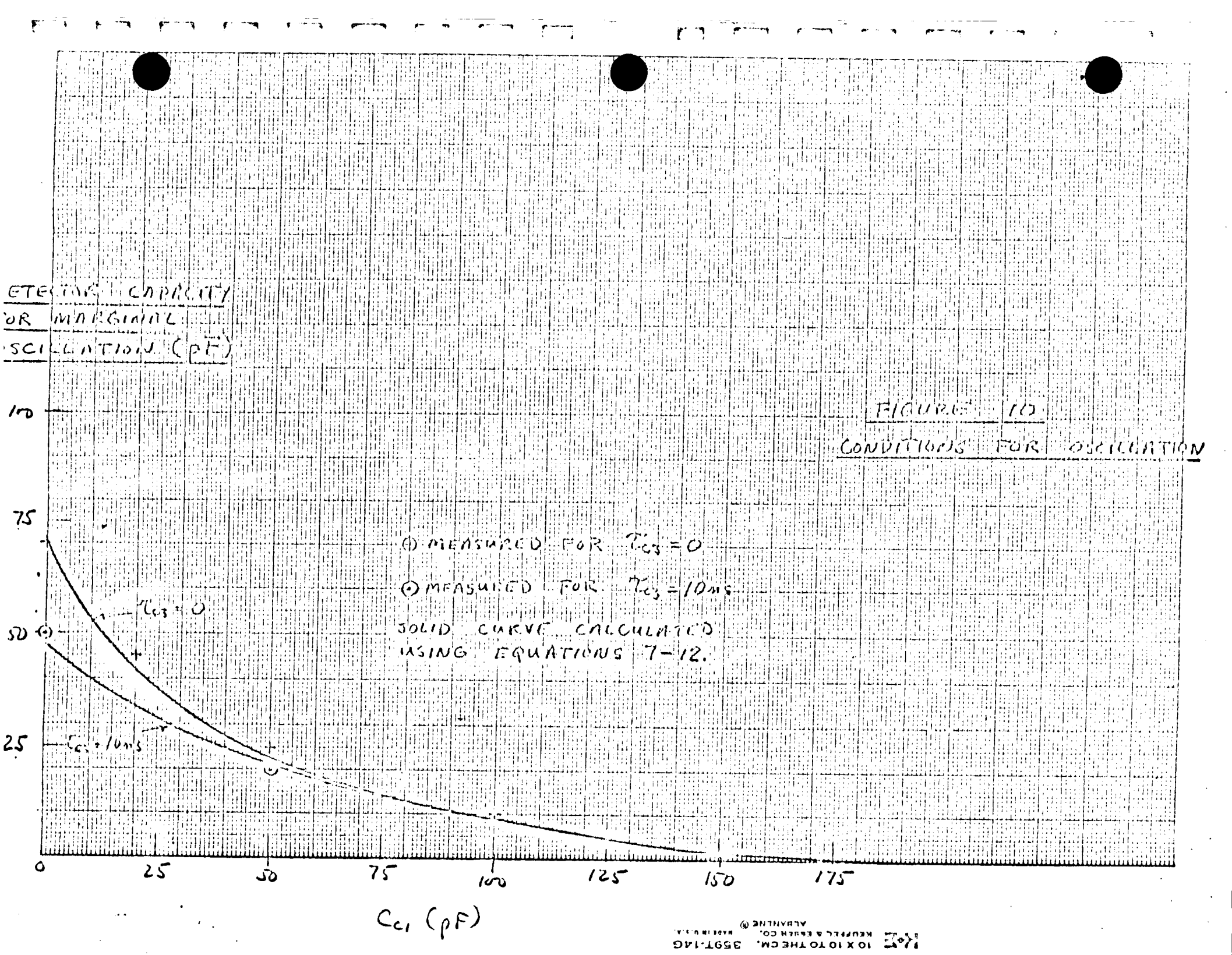
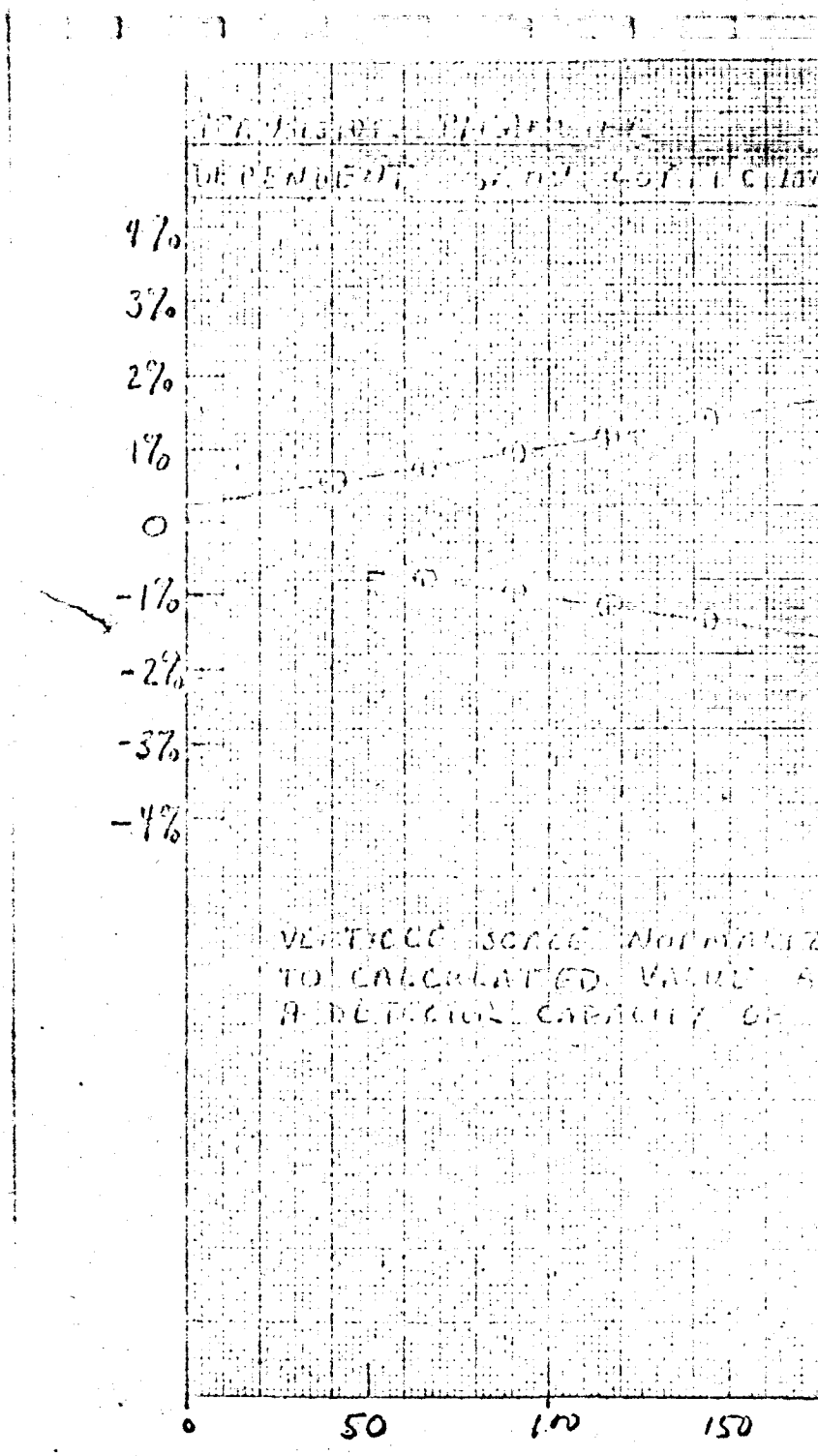


FIGURE 3
ASYMPTOTIC
FEEDBACK FACTOR
100pF
10
1
10^{-1}
10^{-2}
10^{-3}
|F| at
Φ = 180°
C_0 = 1pF
C_{c1} = 500pF
|F| at
Φ = 180°
C_0 = 100pF
C_{c1} = 17.5pF
T = 25°C
1μs
100ns
10ns
1ns
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 5 CYCLES


KEUFFEL & ESSER CO. MADE IN U.S.A.
3 X 5 CYCLES
10
10-2
10-3
10-4
10-5
10-6
ms
10-2 s
10-1 s
s


900
800
CAPACITY IN pF
RESISTANCE IN OHMS
700
600
500
400
300
200
100
0
20
40
60
80
100
200
300
400
500
C_D(pF)
LOAD CAPACITY = 200pF
LOAD RESISTANCE = 1K
R_{C1}
C_{C1}
R_{C3}
FIGURE 9
COMPENSATION VALUES
VS. CAPACITY


ETER CAPACITY
OR MARGINAL
SCILLATION (pF)
100
75
50
25
0
25
50
75
100
125
150
175
C_{c1} (pF)
C_{c3} = 0
C_{c3} = 10ms
⊙ MEASURED FOR C_{c3} = 0
⊙ MEASURED FOR C_{c3} = 10ms
SOLID CURVE CALCULATED USING EQUATIONS 7-12.
FIGURE 10
CONDITIONS FOR OSCILLATION


4%
3%
2%
1%
0
-1%
-2%
-3%
-4%
0
50
100
150

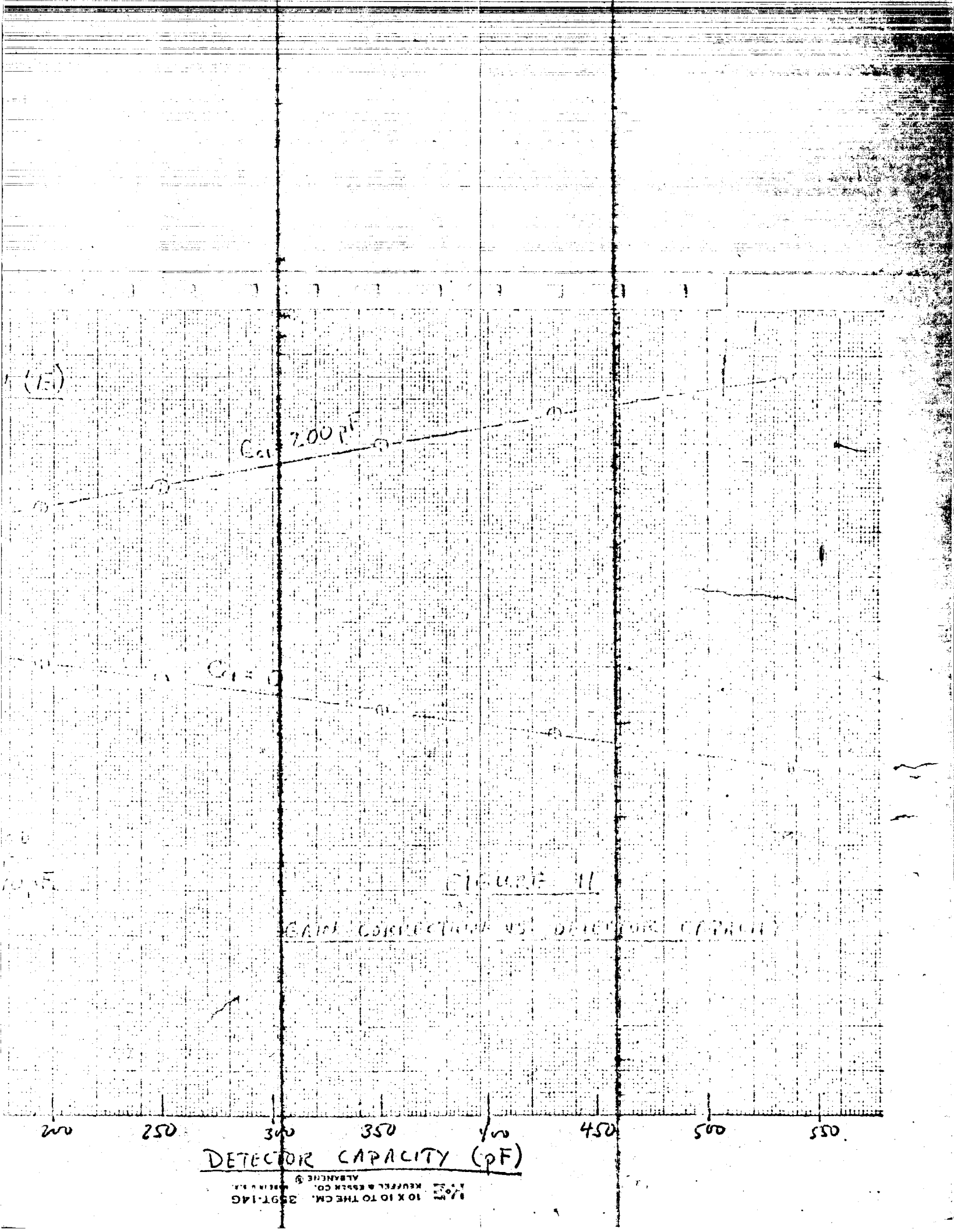
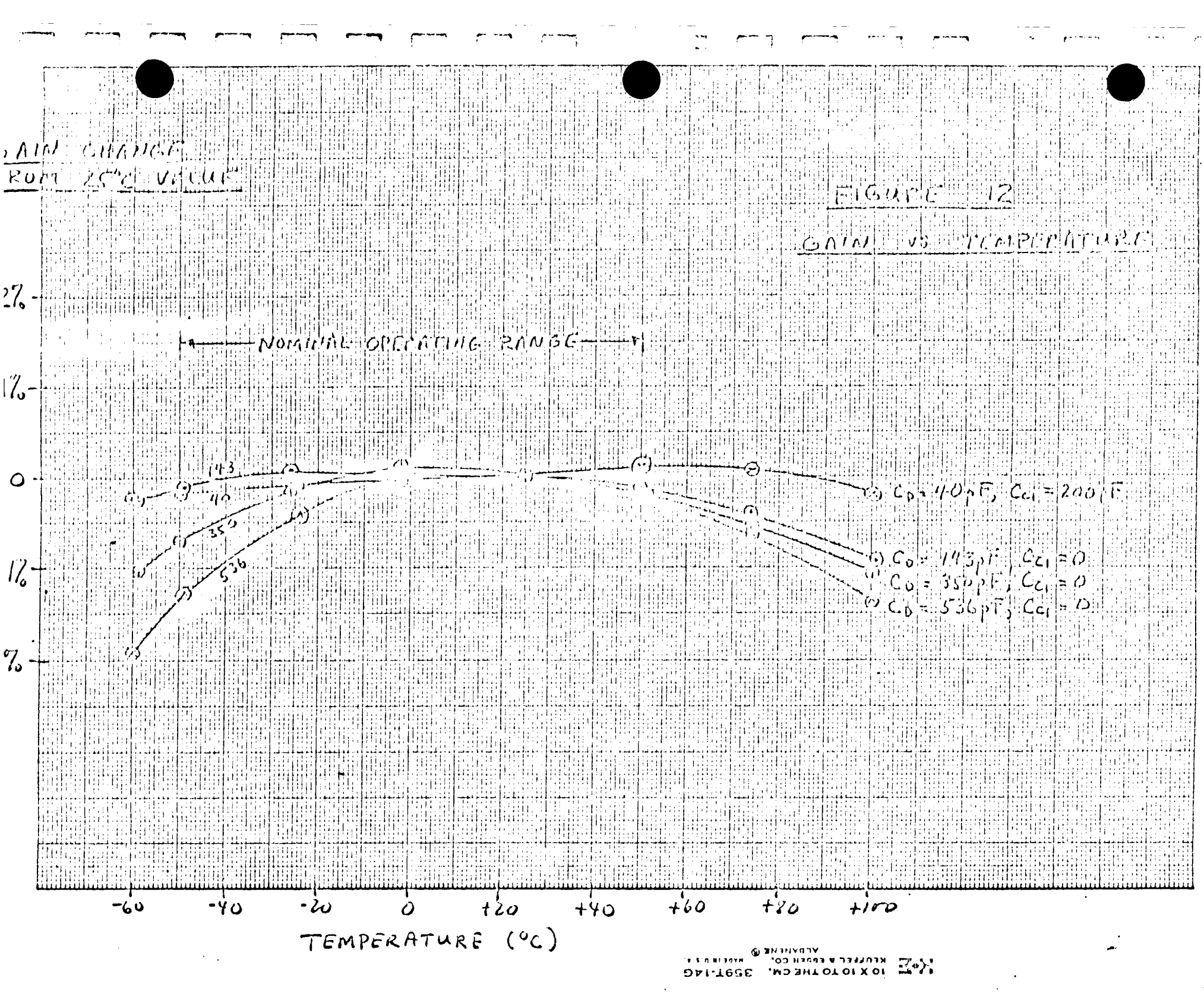
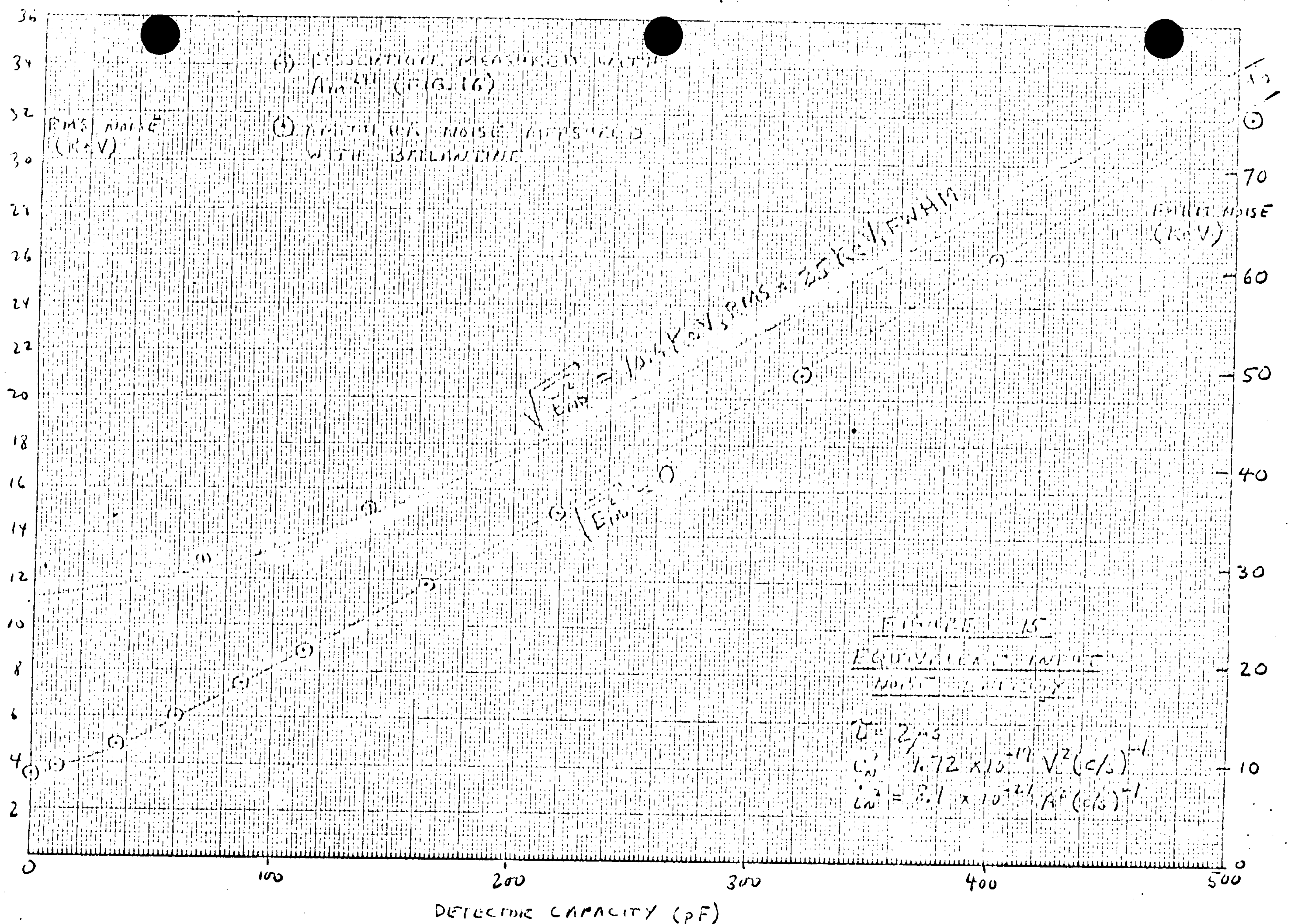


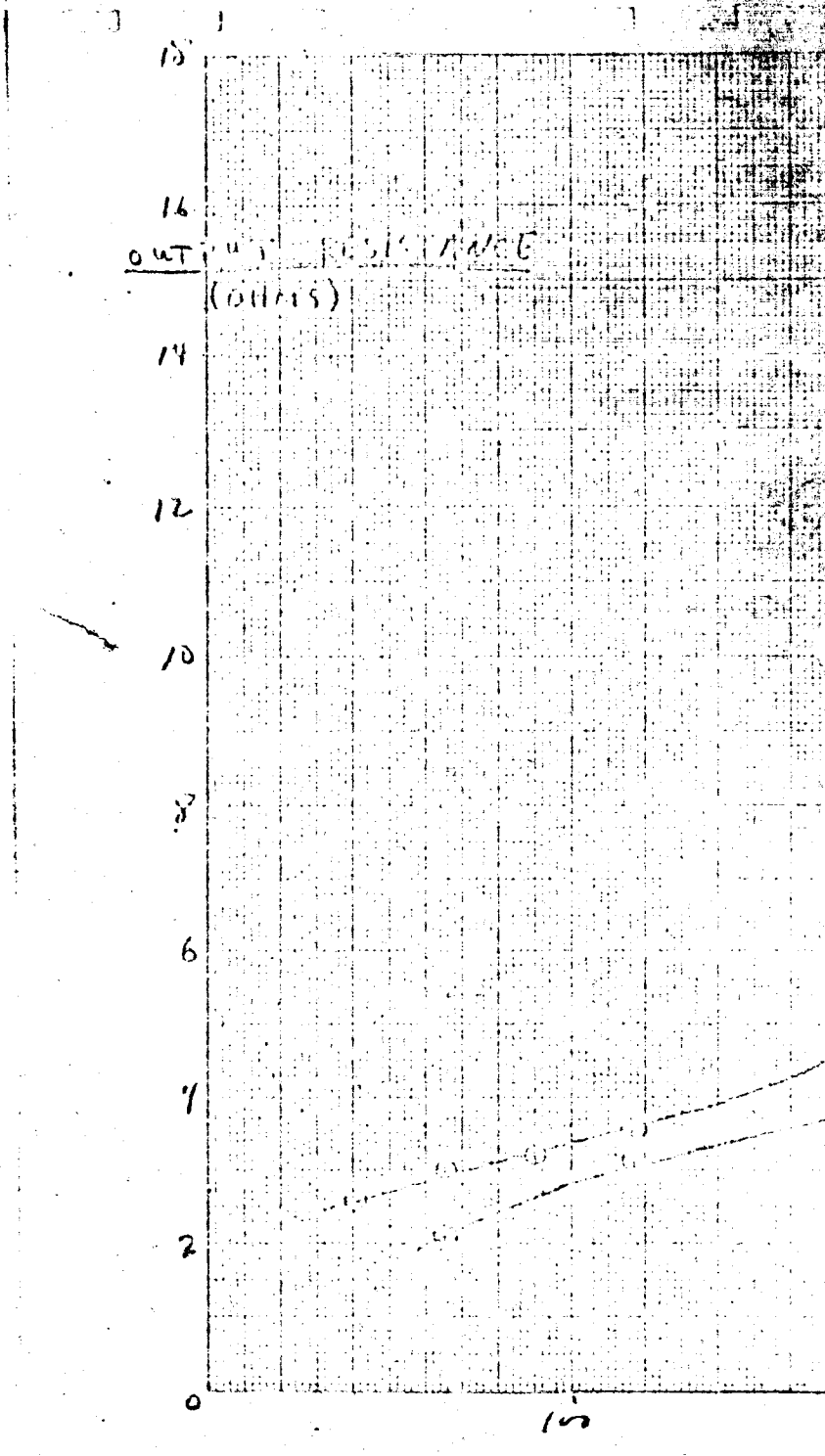
FIGURE 11

GAIN CORRECTION VS. DETECTOR CAPACITY


AIN CHANGE
ROM 25°C VALUE
FIGURE 12
GAIN VS TEMPERATURE
2%
1%
0
1%
%
NOMINAL OPERATING RANGE
143
40
350
536
C_D = 40pF, C_{CI} = 200pF
C_D = 143pF, C_{CI} = 0
C_D = 350pF, C_{CI} = 0
C_D = 536pF, C_{CI} = 0
-60
-40
-20
0
+20
+40
+60
+80
+100
TEMPERATURE (°C)
10 X 10 TO THE CM. 359T-1AG
KEUFFEL & ESSER CO. MADE IN U.S.A.
ALBANENE



RMS NOISE (keV)
FWHM NOISE (keV)
DETECTOR CAPACITY (pF)
FIGURE 15
EQUIVALENT INPUT
NOISE


16
14
12
10
8
6
4
2
0

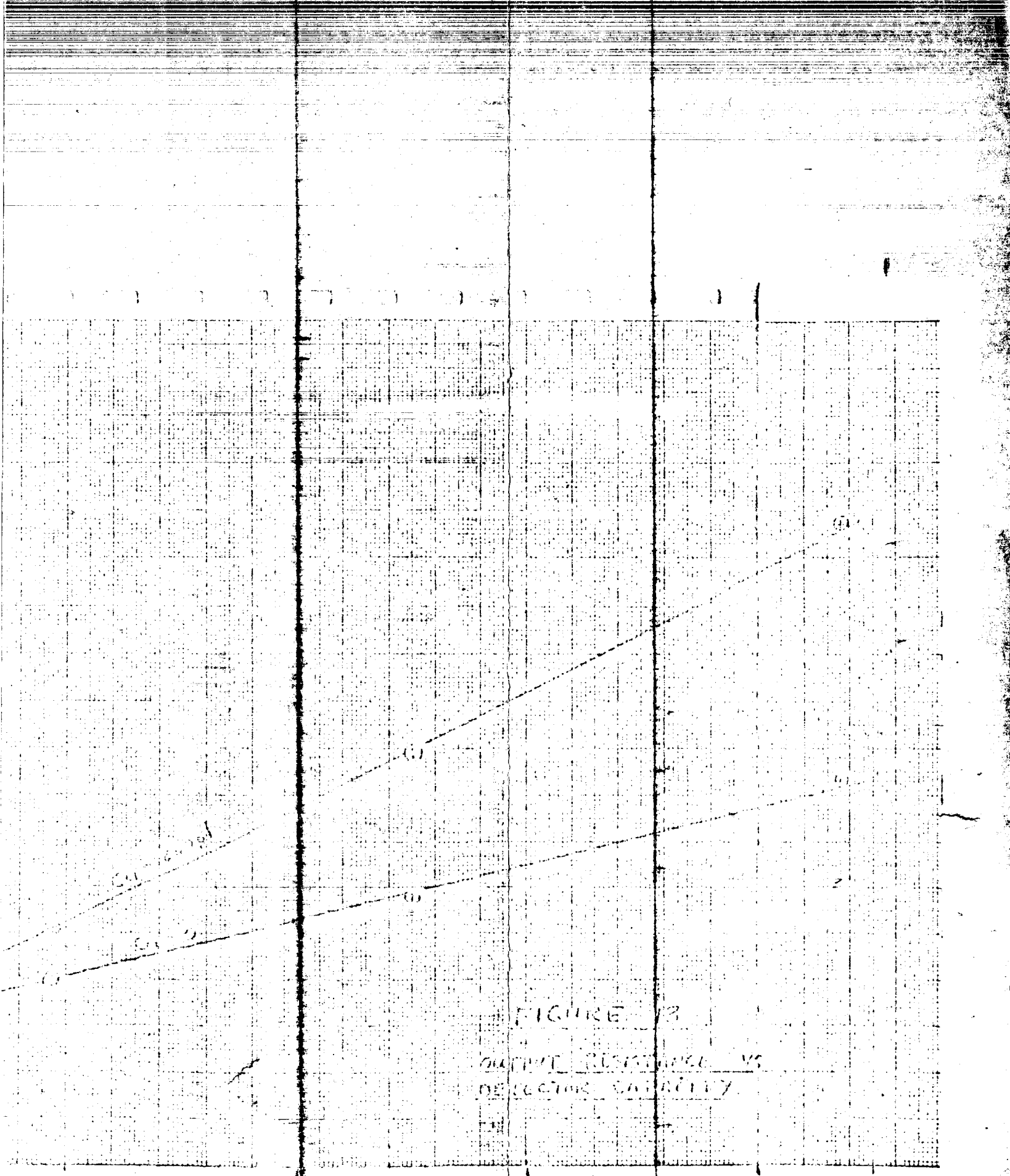


FIGURE 12

OUTPUT RESISTANCE VS
DETECTOR CAPACITY

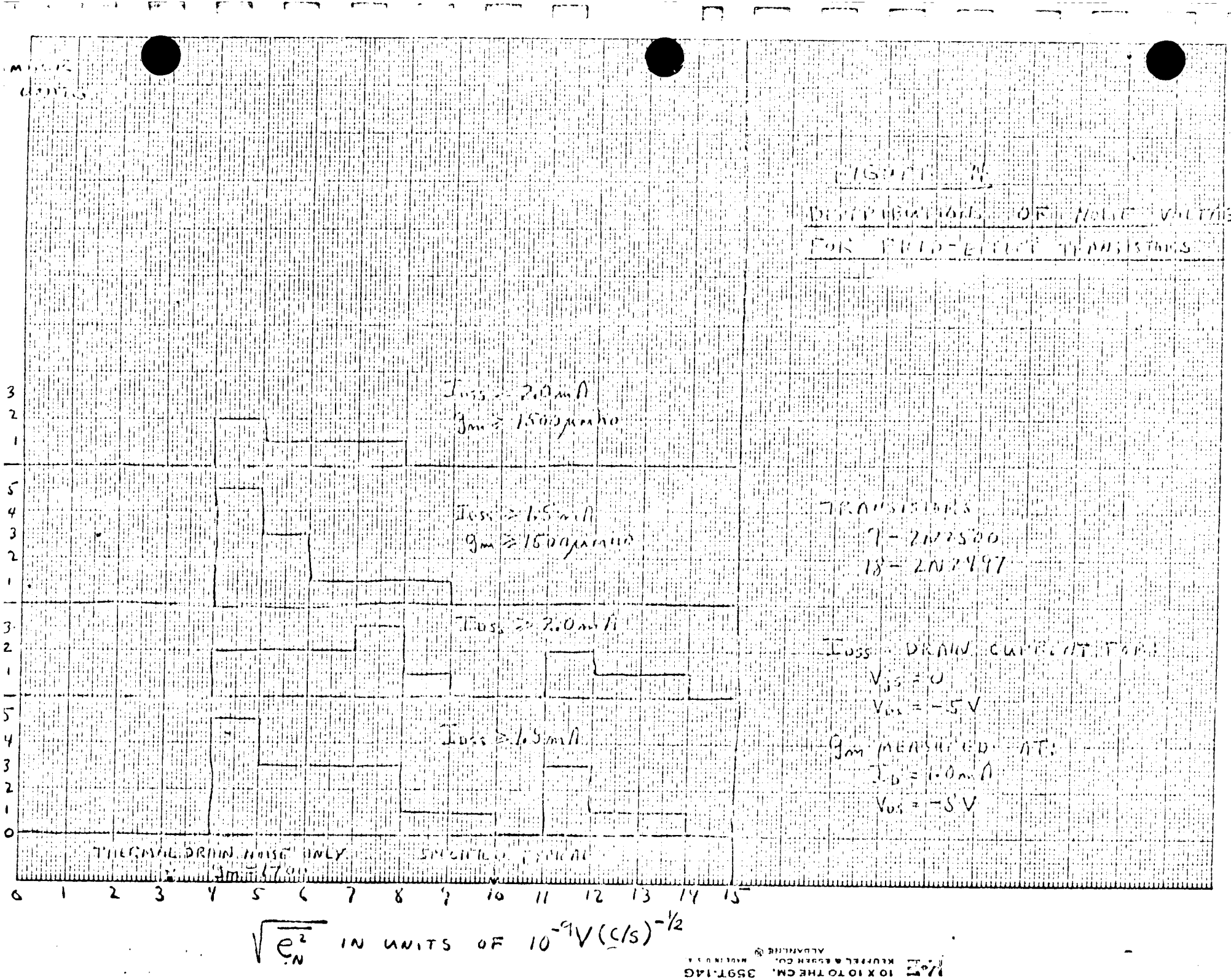


FIGURE 11
DISTRIBUTIONS OF NOISE VOLTAGE
FOR FIELD-EFFECT TRANSISTORS
TRANSISTORS
1 - 2N5500
18 - 2N2497
I_{DSS} - DRAIN CURRENT TEST:
$V_{GS} = 0$
$V_{DS} = -5V$
g_{fs} MEASURED AT:
$I_D = 1.0mA$
$V_{DS} = -5V$
$I_{DSS} = 2.0mA$
$g_{fs} \geq 1500\mu mho$
$I_{DSS} = 1.5mA$
$g_{fs} \geq 1500\mu mho$
$I_{DSS} = 2.0mA$
$I_{DSS} = 1.5mA$
THERMAL DRAIN NOISE ONLY
$\Delta f = 1Kc$
$\sqrt{\overline{e_N^2}}$ IN UNITS OF $10^{-9}V(c/s)^{-1/2}$

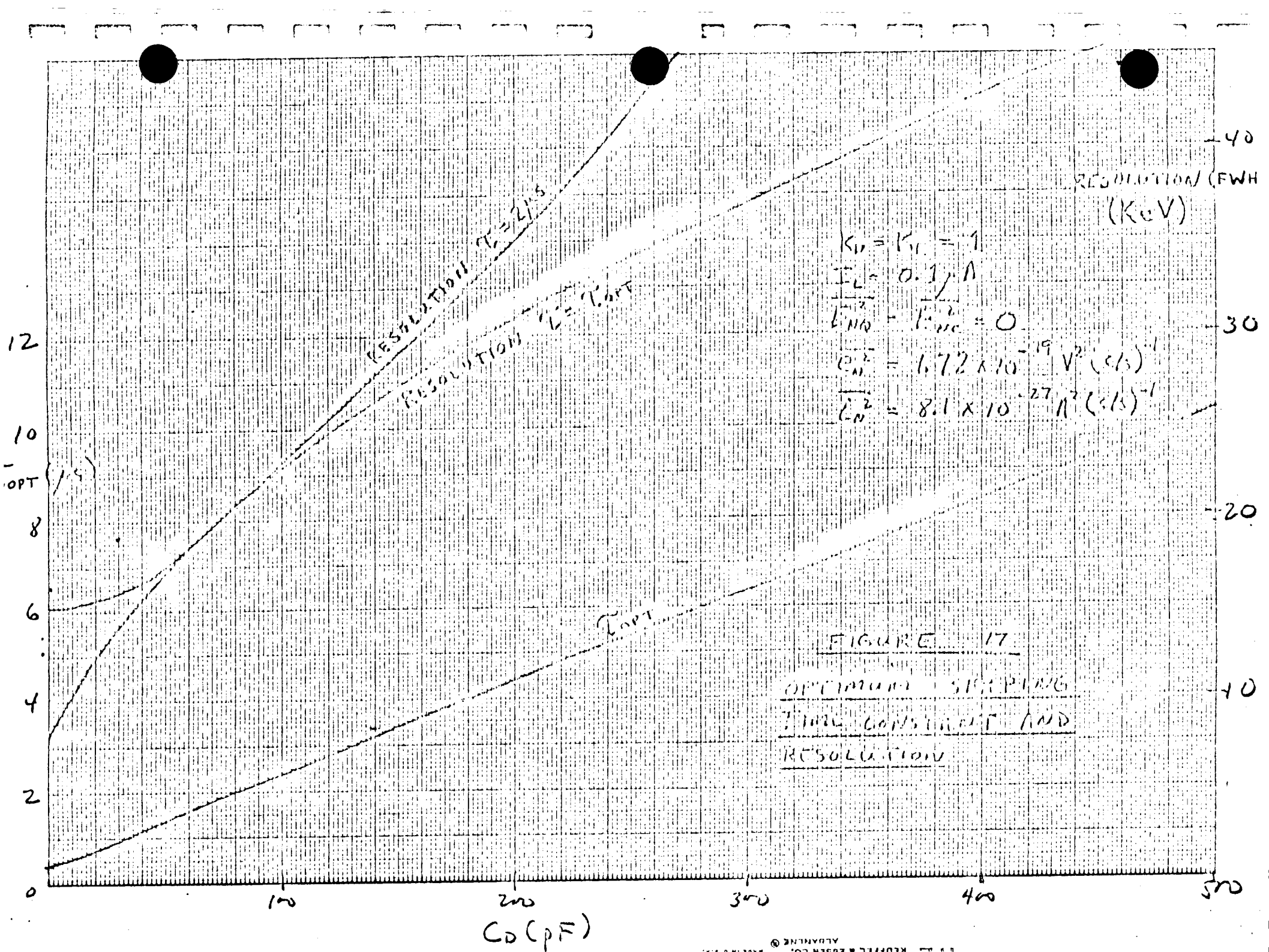
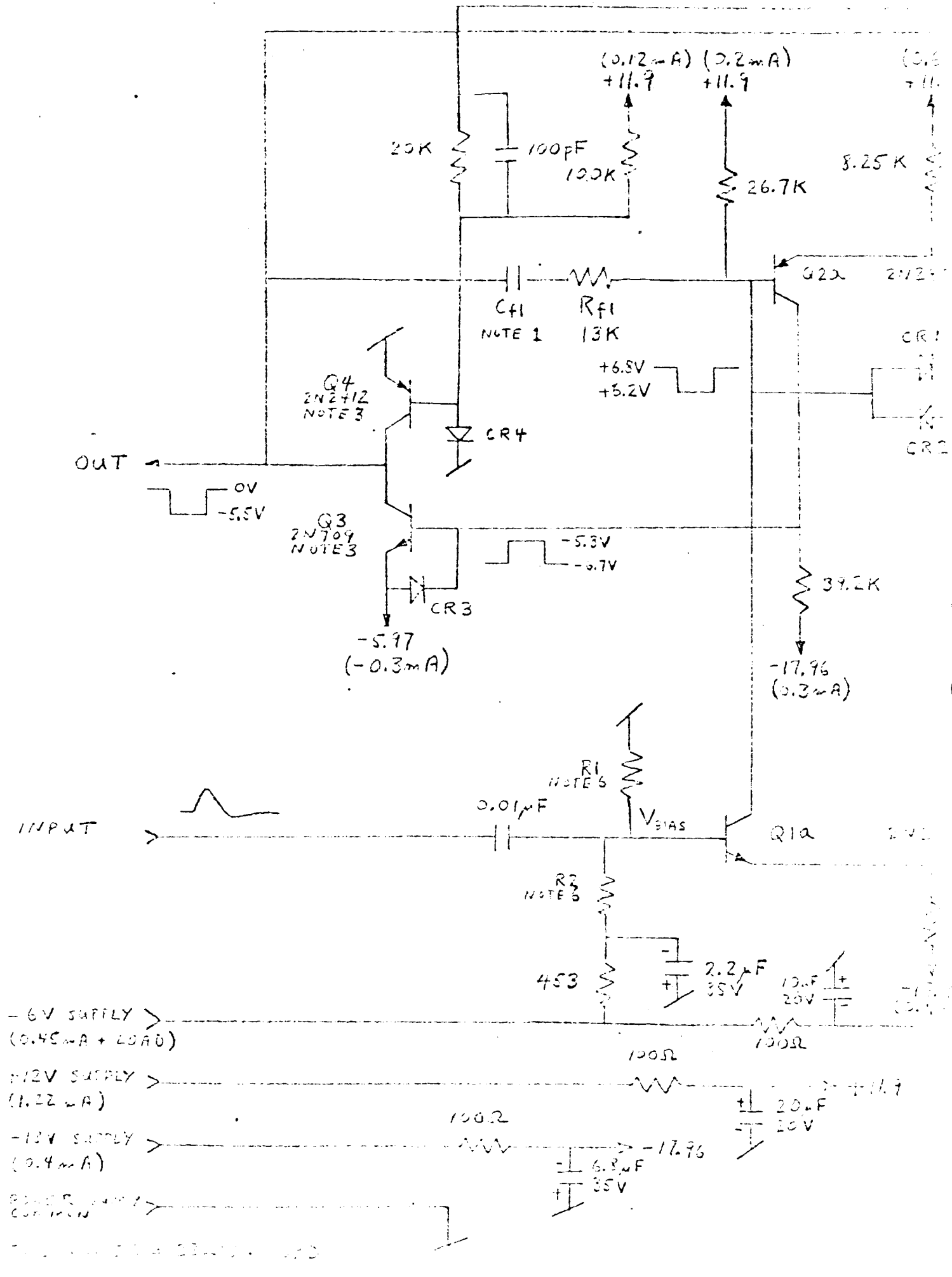
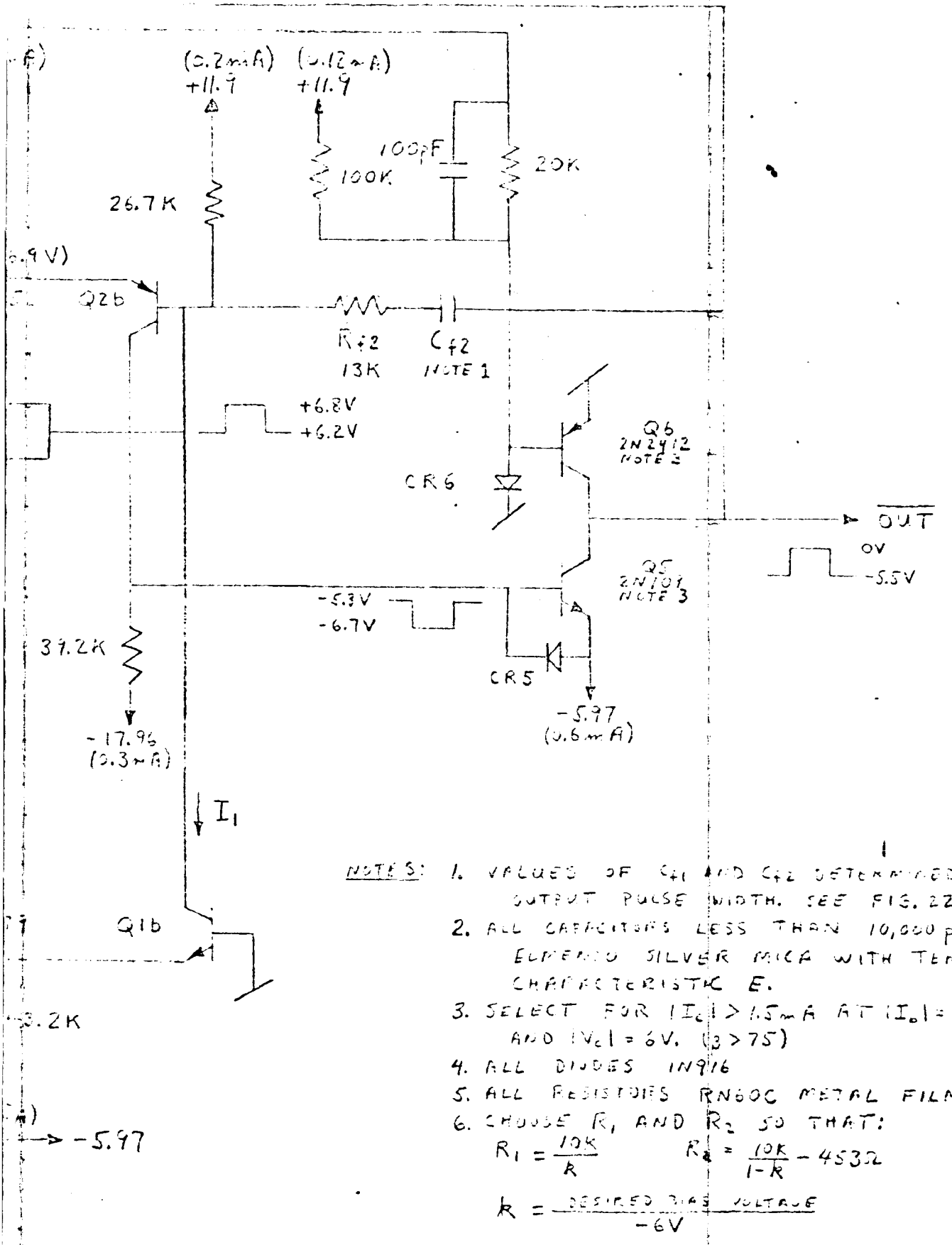


FIGURE 17

OPTIMUM SHAPING TIME CONSTANT AND RESOLUTION


(0.12mA) +11.9
(0.2mA) +11.9
20K
100pF
100K
26.7K
8.25K
Cf1
NOTE 1
Rf1
13K
Q2a
Q4
2N2712
NOTE 3
CR4
+6.5V
+5.2V
CR1
CR2
OUT
0V
-5.5V
Q3
2N709
NOTE 3
-5.3V
-0.7V
CR3
39.2K
-5.97
(-0.3mA)
-17.96
(0.3mA)
R1
NOTE 6
0.01μF
INPUT
VBIAS
Q1a
R2
NOTE 6
453
2.2μF
35V
10μF
20V
-6V SUPPLY
(0.45mA + LOAD)
100Ω
100Ω
+12V SUPPLY
(1.22mA)
20μF
20V
100Ω
-12V SUPPLY
(0.4mA)
-17.96
6.8μF
35V



NOTES:

1. VALUES OF C_{f1} AND C_{f2} DETERMINED BY DESIRED OUTPUT PULSE WIDTH. SEE FIG. 22.
2. ALL CAPACITORS LESS THAN 10,000 pF ARE ELMENCO SILVER MICA WITH TEMPERATURE CHARACTERISTIC E.
3. SELECT FOR $|I_c| > 1.5$mA AT $|I_b| = 0.02$mA AND $|V_c| = 6$V. ($\beta > 75$)
4. ALL DIODES IN916
5. ALL RESISTORS RN60C METAL FILM
6. CHOOSE R_1 AND R_2 SO THAT:

$$R_1 = \frac{10K}{k} \qquad R_2 = \frac{10K}{1-k} - 4532$$

$$k = \frac{\text{DESIRED BIAS VOLTAGE}}{-6V}$$

FIGURE 17

DISCRIMINATOR

SCHEMATIC

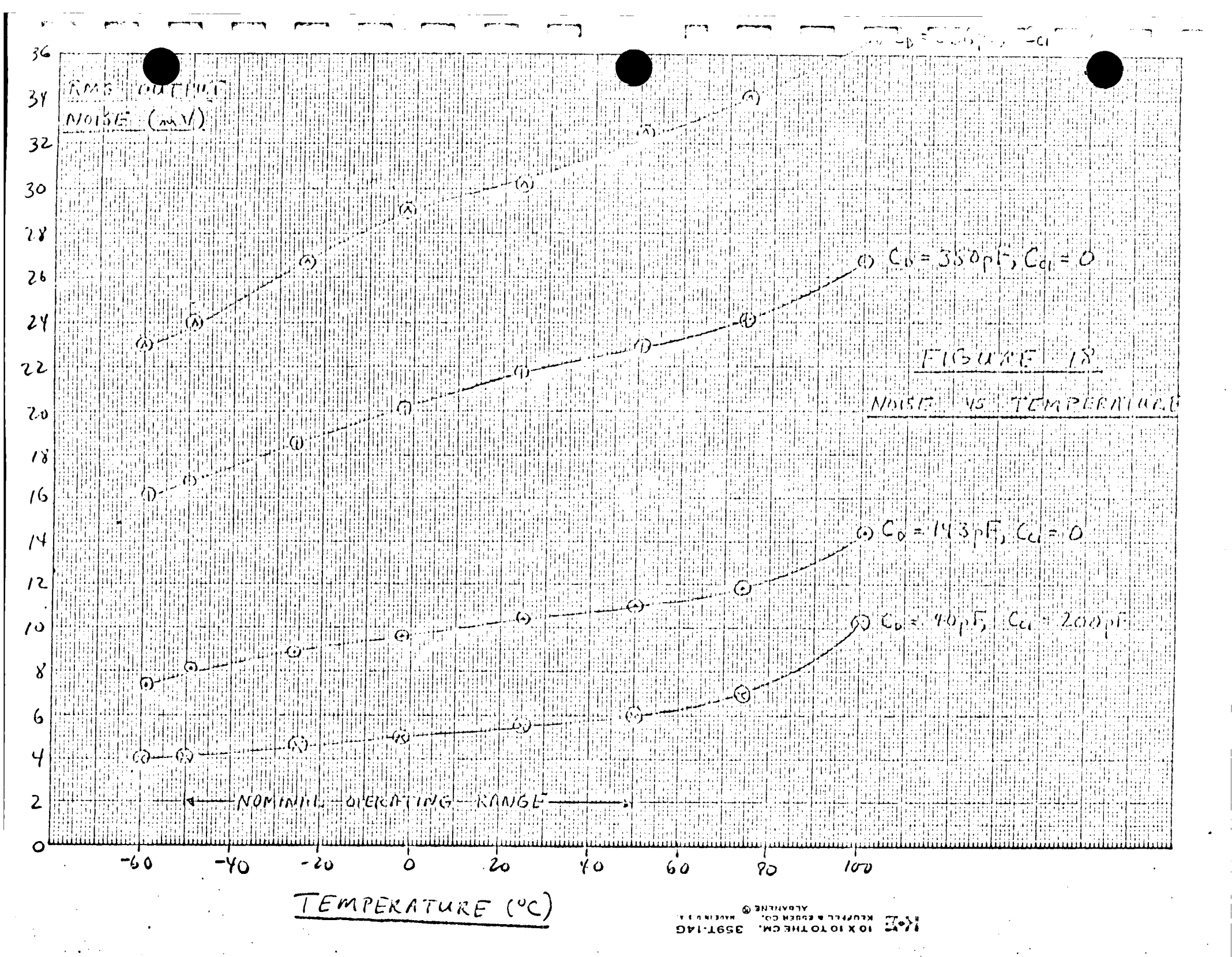


FIGURE 18

NOISE VS TEMPERATURE

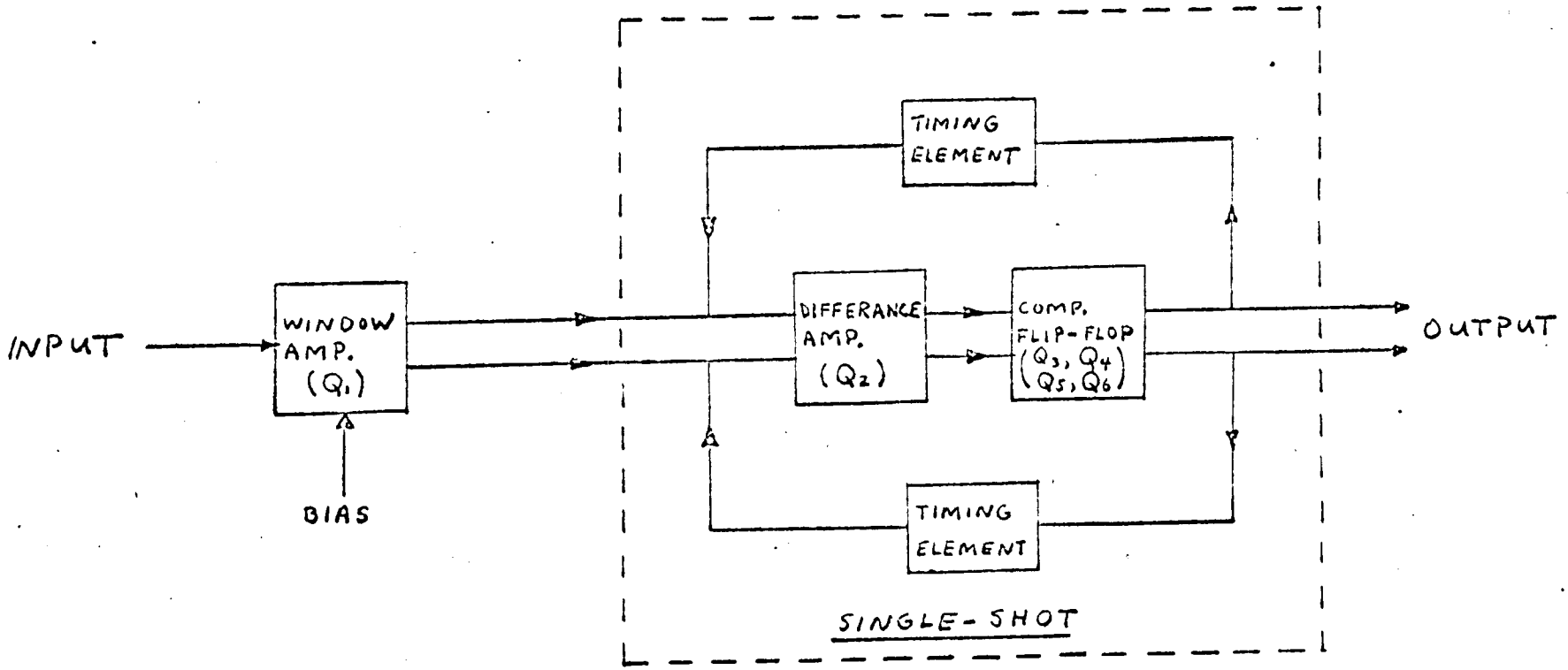


FIGURE 20
DISCRIMINATOR
BLOCK DIAGRAM

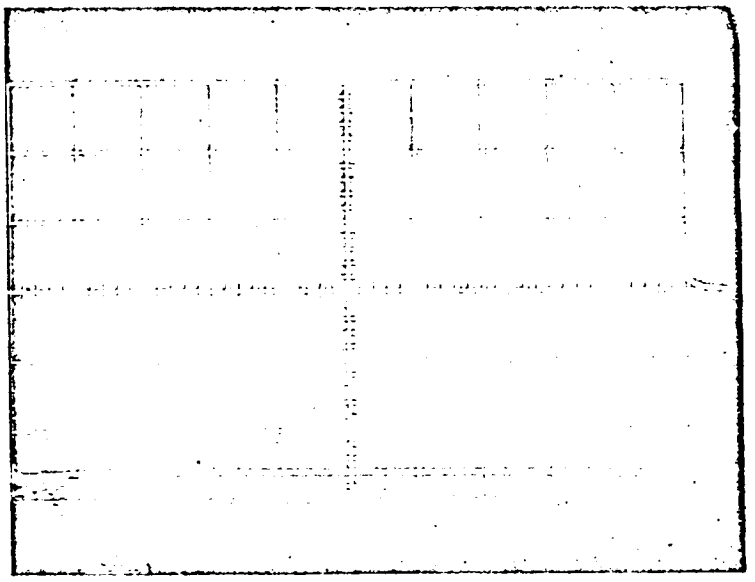
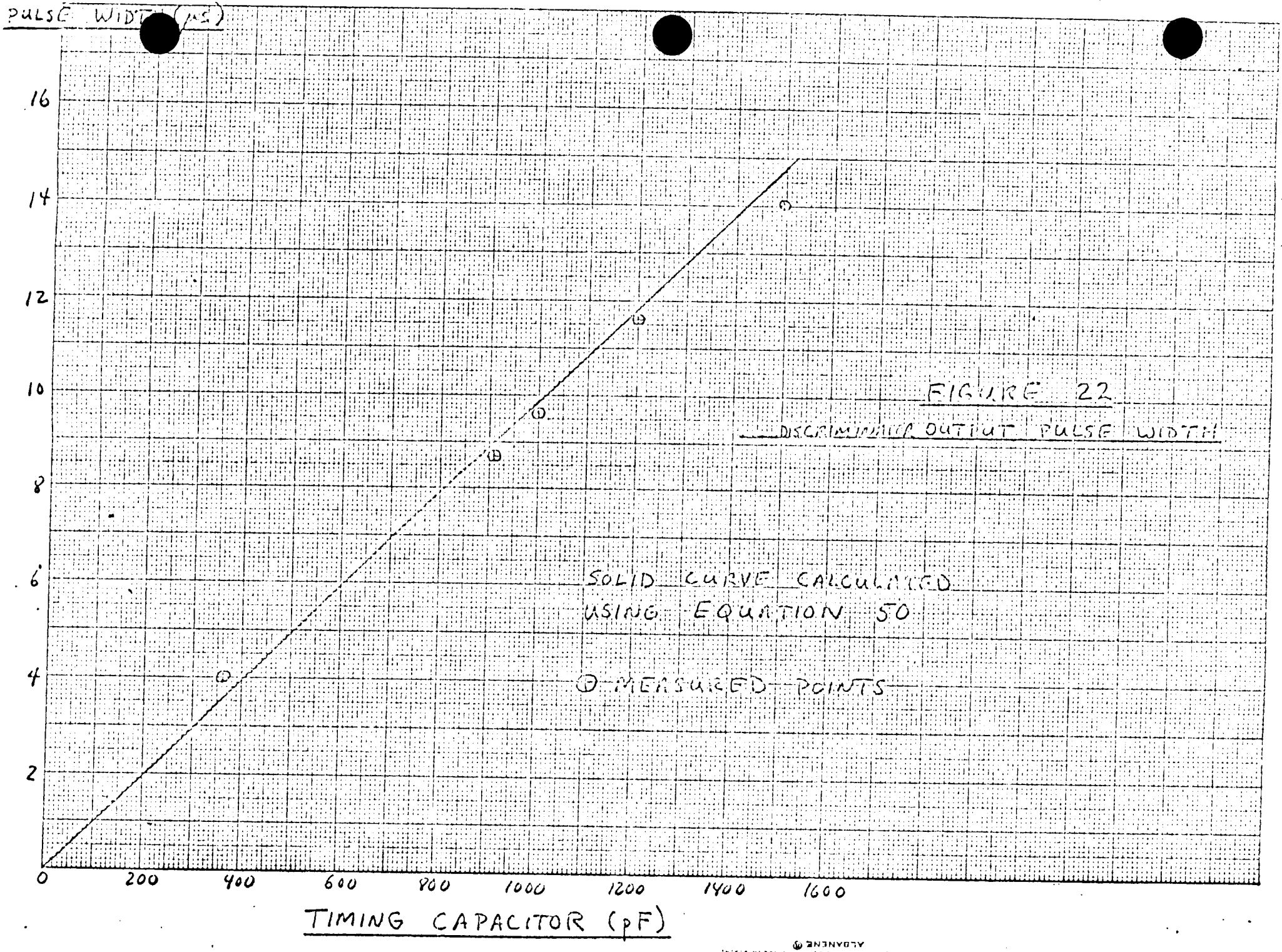


Fig. 21 - Discriminator Output Pulse

Horizontal: 1μs/cm
Verticle: 2.1V/cm



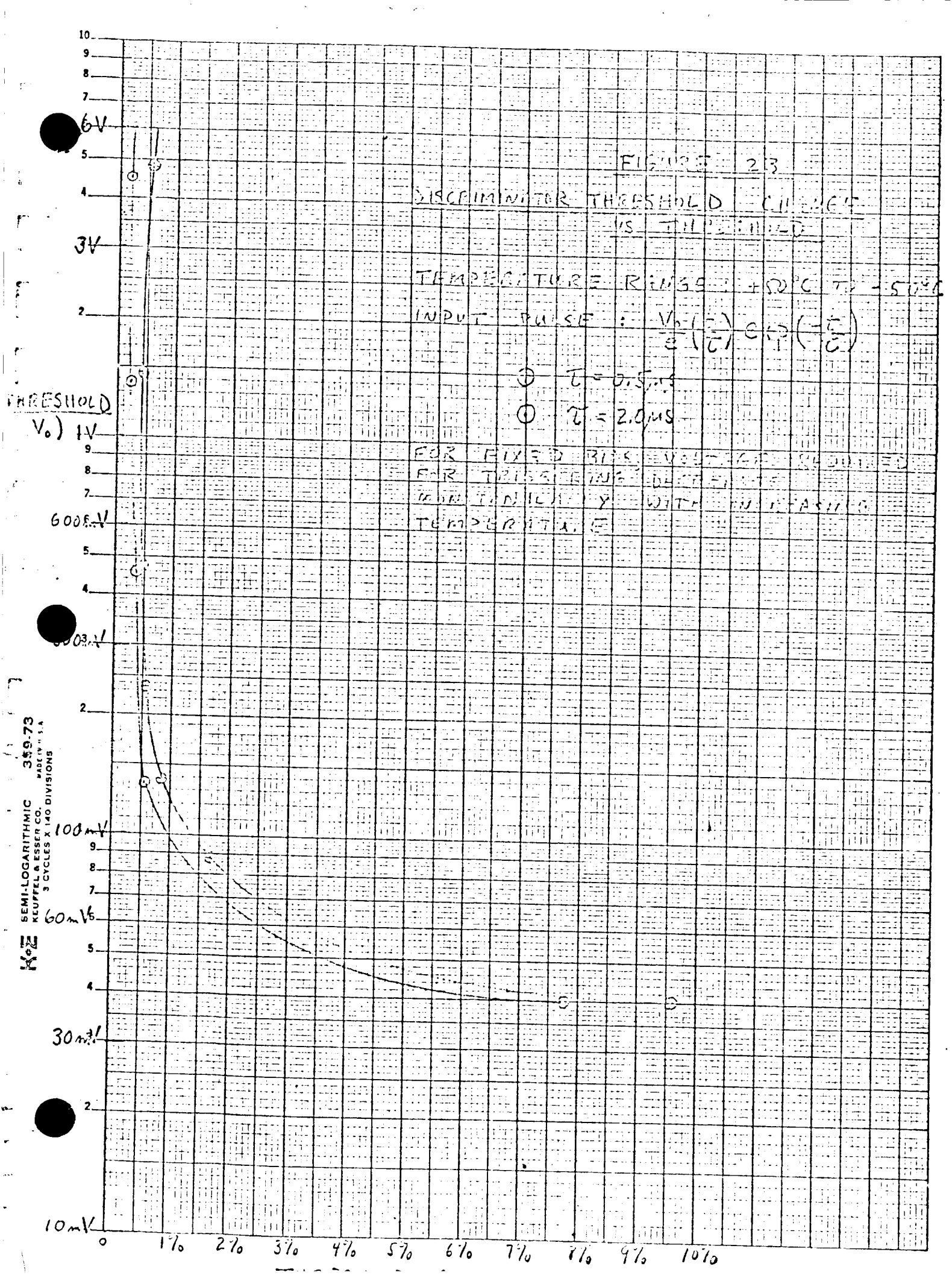


FIGURE 23
DISCRIMINATOR THRESHOLD CHANGE VS TEMPERATURE
TEMPERATURE RANGE: +80°C TO -55°C
INPUT PULSE: $V_0\left(\frac{-t}{C}\right) e^{+}\left(\frac{-t}{C}\right)$
τ = 0.5 μs
τ = 2.0 μs
FOR FIXED RISE TIME AND DELAY
FOR TRIGGERING DEVICE
RISE TIME VARIATION
TEMPERATURE
THRESHOLD
V_0) 1V
600mV
300mV
100mV
60mV
30mV
10mV
6V
3V
0
1%
2%
3%
4%
5%
6%
7%
8%
9%
10%
SEMI-LOGARITHMIC 359-73
KEUFFEL & ESSER CO. MADE IN U.S.A.
3 CYCLES X 140 DIVISIONS
KE